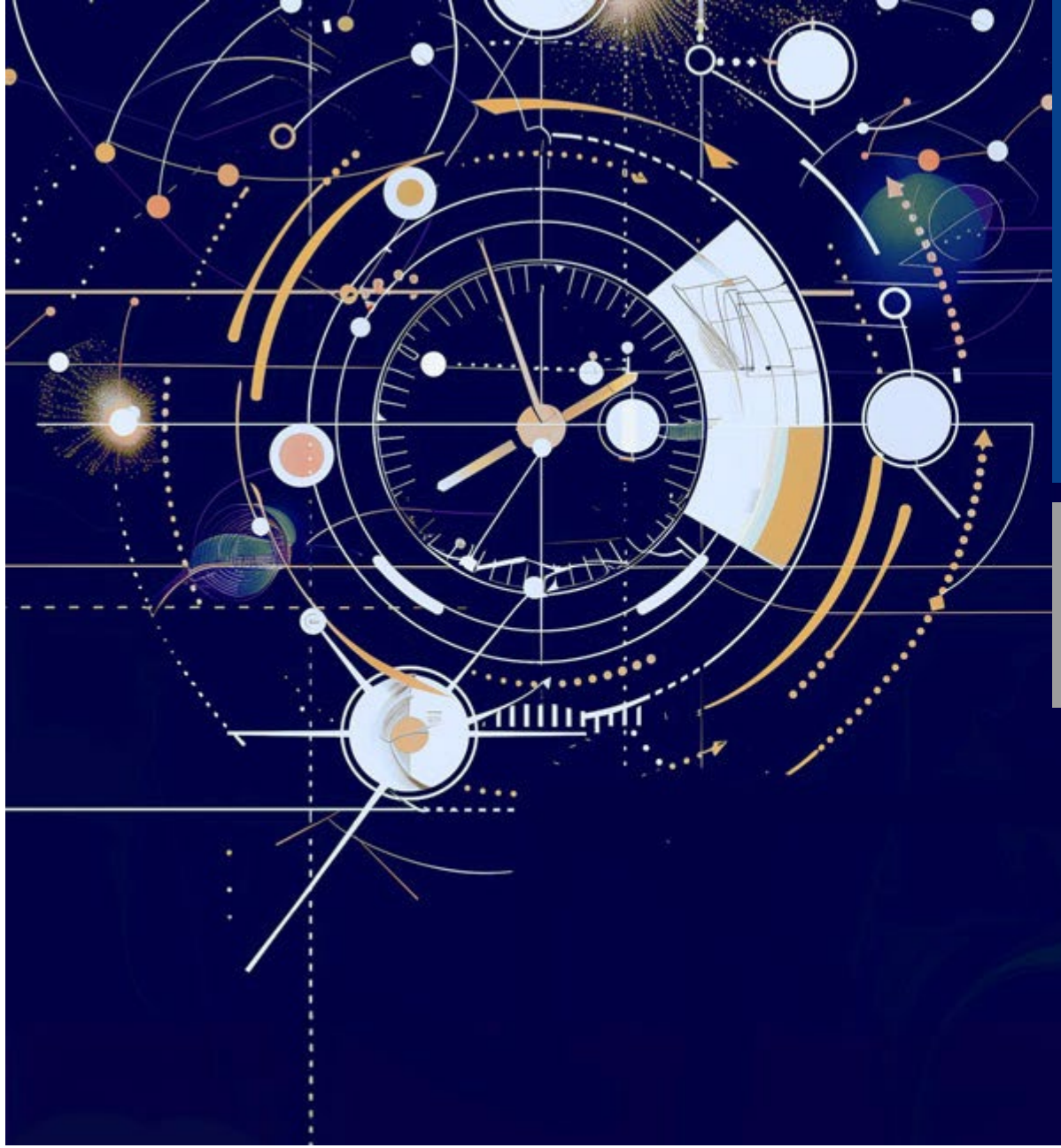


EPPSILON AT THE EDGE

EPPS PRECISION FOR RESILIENT TIMING

GREG ARMSTRONG
PRINCIPAL SYSTEM ARCHITECT, TIMING DIVISION
RENESAS ELECTRONICS CORPORATION

WORKSHOP
ON
SYNCHRONIZATION
AND
TIMING SYSTEMS

EDGE AI & AUTONOMOUS SYSTEMS DEMAND SUB-NS TIMING

Need for Precise Timing

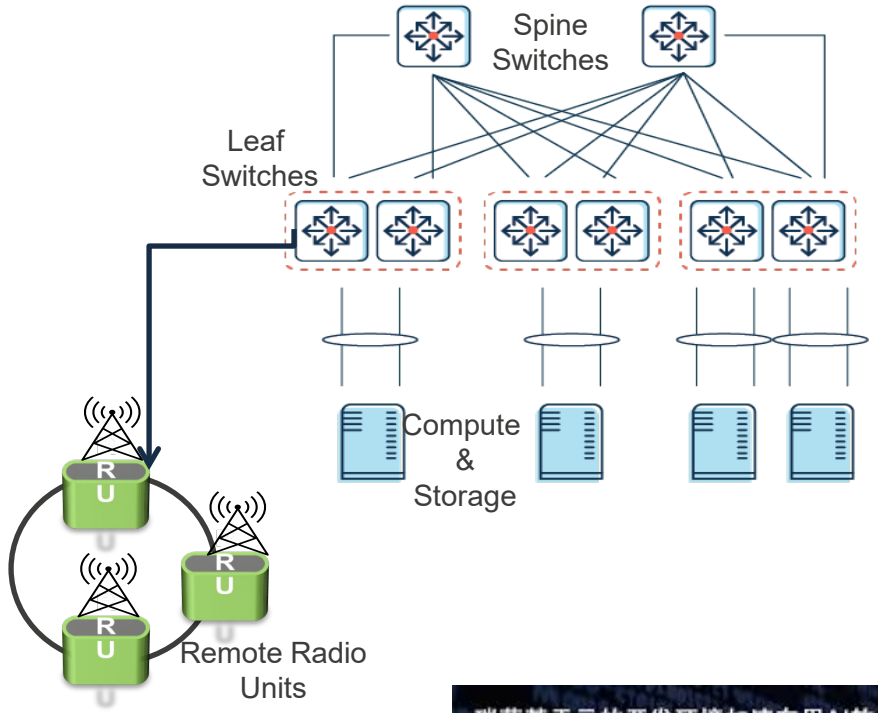
Sub-nanosecond synchronization is critical for Telecom, AI, and autonomous systems to ensure accuracy and stable operations.

Challenges of Traditional Timing

Existing timing methods using separate frequency and pulse signals face physical and signal-integrity challenges at the edge.

Unified Timing Approach

A combined method for phase and frequency transport is needed to meet timing precision within modern edge hardware constraints.



LIMITATIONS OF TRADITIONAL 10 MHZ AND STANDALONE 1PPS DISTRIBUTION

Separate Frequency and Phase Signals

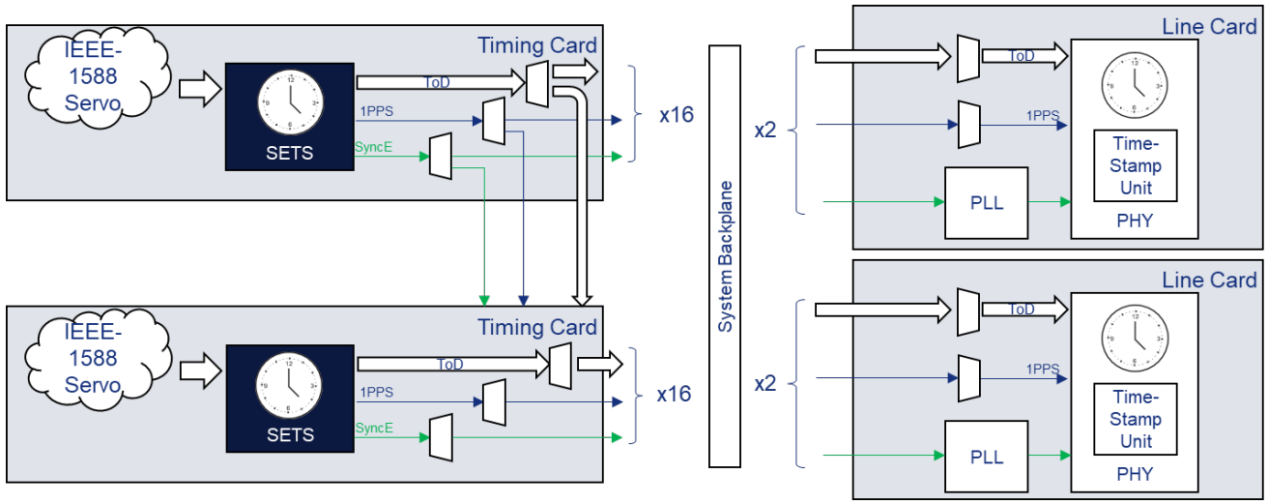
Traditional timing distribution uses distinct 10 MHz frequency and 1PPS phase signals, increasing routing complexity and cost.Trace/Cable length and connector variations introduce skew and jitter, complicating sub-nanosecond alignment in dense systems.

Interface Pin Limitations

Standard interfaces and backplanes have limited pins, making separate 10 MHz and 1PPS signals impractical, hindering interoperability.

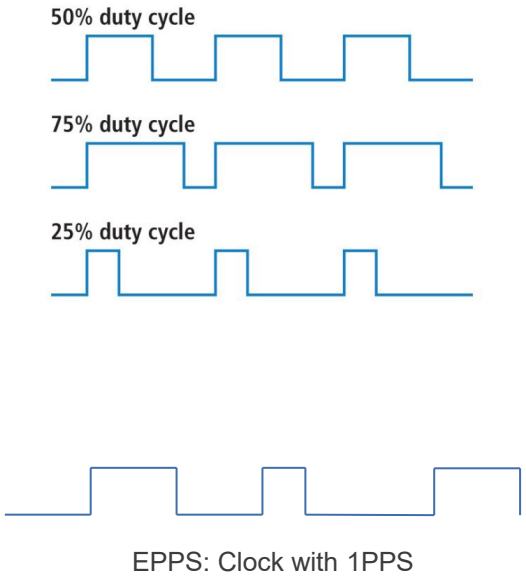
Need for Integrated Timing Method

A unified signal conveying frequency and phase reduces skew, simplifies routing, and suits modern compute platforms.



EMBEDDED PULSE-PER-SECOND (EPPS) CONCEPT

EMBEDDING 1PPS INTO A 10 MHZ CLOCK USING DUTY-CYCLE MODULATION



EPPS: Clock with 1PPS

Duty-Cycle Modulation Technique

EPPS embeds a 25% duty cycle pulse at the 1PPS boundary within the 10 MHz clock signal, leaving other cycles at 50%.

Phase and Frequency Alignment

Embedding PPS markers ensures intrinsic alignment of frequency and phase, eliminating ambiguity from separate signals.

Detection and Recovery

Detection uses comparator logic or digital sampling followed by DPLL to recover continuous frequency and discrete time.

Standards Compliance and Benefits

EPPS carrier complies with ITU-T G.703, reducing cabling and skew while enabling synchronized timing distribution.

ELECTRICAL PERFORMANCE AND COMPLIANCE CHARACTERISTICS OF EPPS

Precision Timing Performance

EPPS achieves sub-nanoseconds alignment and jitter below 100 picoseconds for highly accurate* signal timing.

Signal Integrity on Short Runs

Validated on short 3-meter copper cables, EPPS maintains signal integrity suitable for edge and rack environments.

Electrical Compliance

EPPS complies with ITU-T G.703 standards for 10MHz clock distribution; but using duty-cycle modulation to avoid interference with adjacent systems.

Focus on Timing Distribution

EPPS distributes precise timing from primary sources like GNSS & PTP without replacing them.

* Measured under controlled short-reach conditions; system-level performance depends on the downstream DPLL and reference quality.

ITU-T G.703 ANNEX PROPOSAL: EXTENDING A PROVEN PHYSICAL LAYER

Building on G.703 Foundation

EPPS extends the established G.703 physical interface by embedding a PPS marker within the 10 MHz signal to enable precise phase distribution.

Backward Compatibility and Adoption

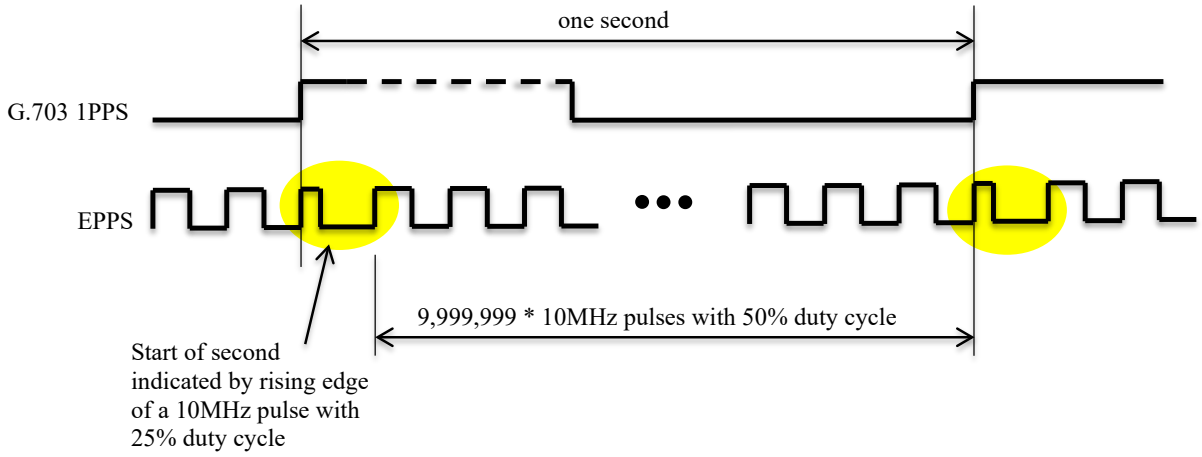
EPPS maintains backward compatibility allowing legacy systems to operate normally while enabling new devices to access phase information.

Unified Timing for Diverse Industries

Proposed Annex provides a standardized, robust solution for precise timing needed across telecom, edge computing, and AI infrastructure.

Practical and Scalable Solution

Embedding precise phase distribution within G.703 positions EPPS as a practical, scalable physical layer standard rather than a niche technique.



EPPS IN EDGE COMPUTING ENVIRONMENTS

DETERMINISTIC TIMING DISTRIBUTION FOR DENSE EDGE PLATFORMS

EPPS for Precise Timing

EPPS distributes precise timing deterministically at the physical layer without protocol overhead or complex software.

Compatibility with Compact Hardware

EPPS works with short copper interconnects and compact routing, simplifying system calibration and bring-up.

Sub-nanosecond Synchronization

Feeding DPLLs with EPPS enables sub-nanosecond frequency and phase accuracy for synchronized heterogeneous components.

Enabling Edge Timing Architectures

EPPS reduces signal complexity and jitter, enabling high-quality timing in dense edge environments beyond telecom.

DEPLOYMENT CONTEXT AND APPLICABILITY

Current usage in modern NIC architectures

Centralized reference-clock distribution is already common in high-performance NIC designs.

OCP NIC 3.0 systems rely on a shared timing source distributed to multiple functional blocks (SerDes, MAC, PHY), rather than fully independent local oscillators.

Relevance to emerging interconnect standards

Increasing data rates and tighter timing margins make reference-clock quality and distribution critical at the system level.

This work naturally aligns with future platforms such as PCI-SIG CEM 7.0, where link performance, retimer behavior, and margining are increasingly sensitive to clock integrity.

Internal system adoption

Similar centralized clock-distribution approaches are already used within complex systems for internal timing and frequency distribution, including intra-card and intra-chassis architectures.

This work characterizes and quantifies the behavior and limitations of such architectures, rather than proposing a new deployment model.

PCI-SIG CEM 7.0 AND OCP NIC 3.0: TIMING INSIDE THE SERVER

FlexIO Pin Repurposing

Legacy JTAG pins were repurposed to FlexIO and later allocated for functions including USB 2.0 and timing synchronization.

Timing Synchronization Interface

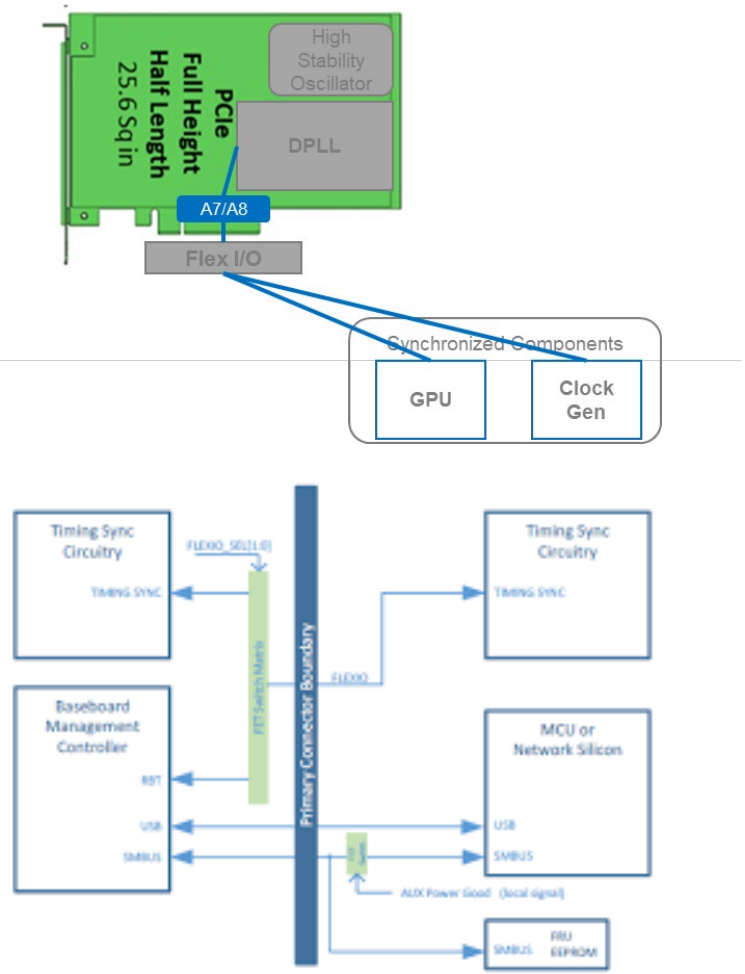
PCI-SIG CEM 7.0 includes provisions for timing synchronization on FlexIO pins, enabling bi-directional timing signal distribution inside servers.

Importance for GPU and Accelerators

Sub-nanosecond timing improves coordination between NICs, CPUs, and accelerators on GPU-heavy platforms.

OCP NIC 3.0 Timing Support

OCP NIC 3.0 already defines FlexIO usage for frequency, phase, and time synchronization supporting telecom and cloud needs.



A UNIFIED FRAMEWORK FOR PRECISE TIMING DISTRIBUTION AT THE EDGE

Unified Timing Framework

EPPS creates a unified timing framework using high-quality precision sources already deployed in modern NIC, edge-compute, and AI accelerator systems.

Physical Layer Transport

EPPS embeds phase information in frequency signals, enabling efficient timing distribution across platforms and devices where centralized reference clocks are already used.

Standardized Interface Integration

Standard interfaces such as OCP NIC 3.0 and PCI-SIG CEM (including emerging CEM 7.0 systems) enable EPPS distribution over existing FlexIO and reference-clock pins, without requiring proprietary links or additional cabling.

System Coherence and Synchronization

By leveraging deployed clock-distribution architectures, EPPS enables sub-nanosecond synchronization and reduces integration risk across diverse systems, topologies, and scaling generations.

Thank You!

Timing is the heartbeat of the system