UC San Diego
JACOBS SCHOOL OF ENGINEERING
Electrical and Computer Engineering

Clock Drift Estimation using Carrier Frequency Offset in 802.11 Networks

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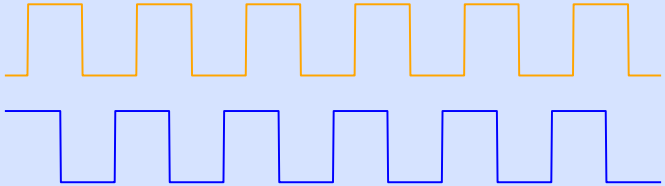
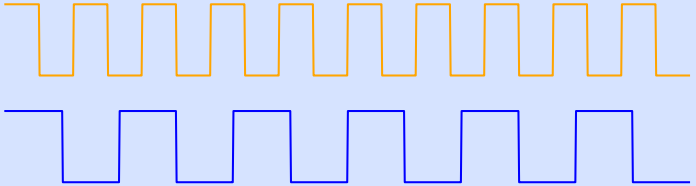
Wireless Synchronization - Why do we want it?

Requirements for a synchronization system

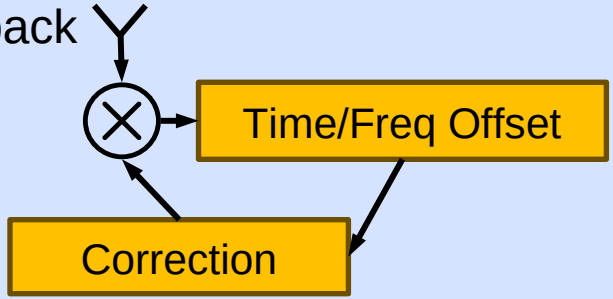
Time Offset Estimation



Frequency Source

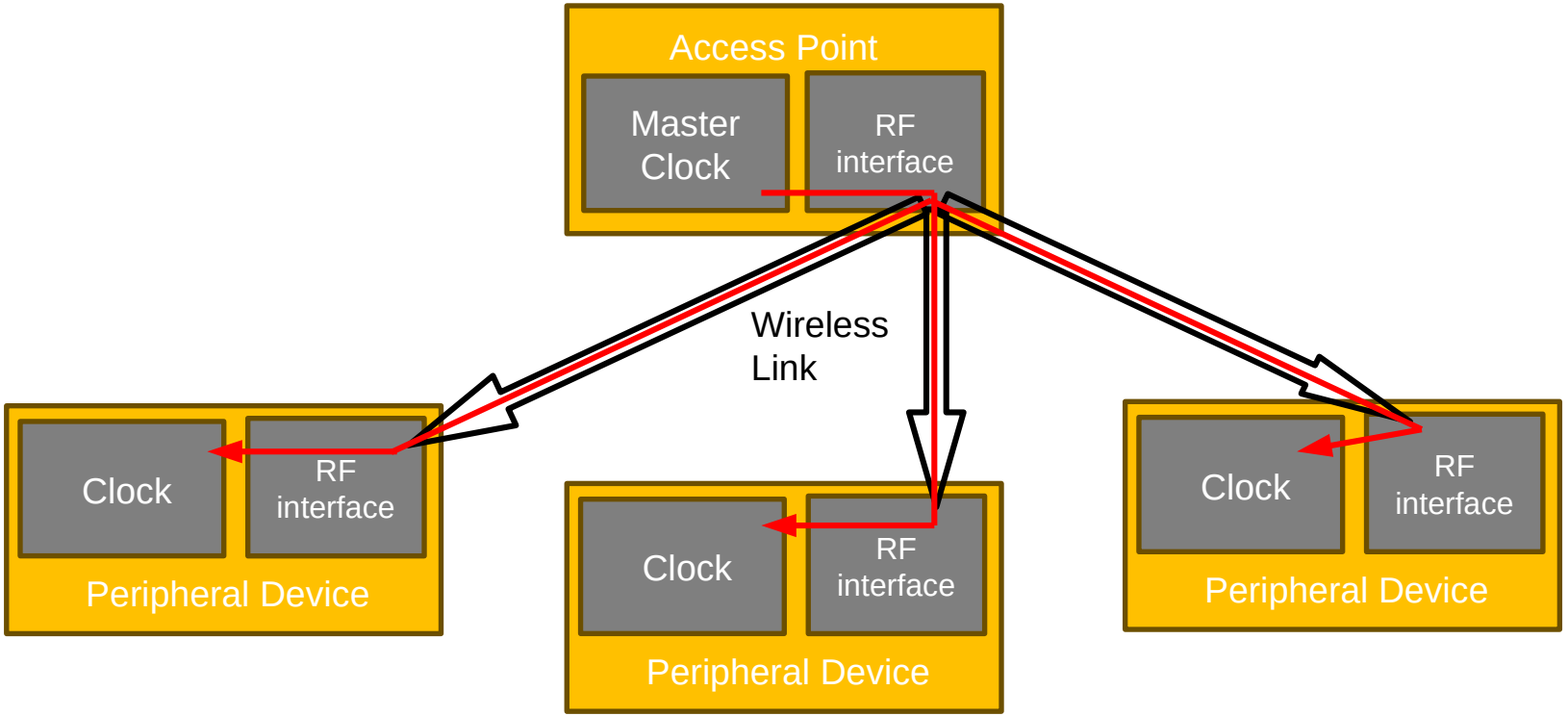


Feedback

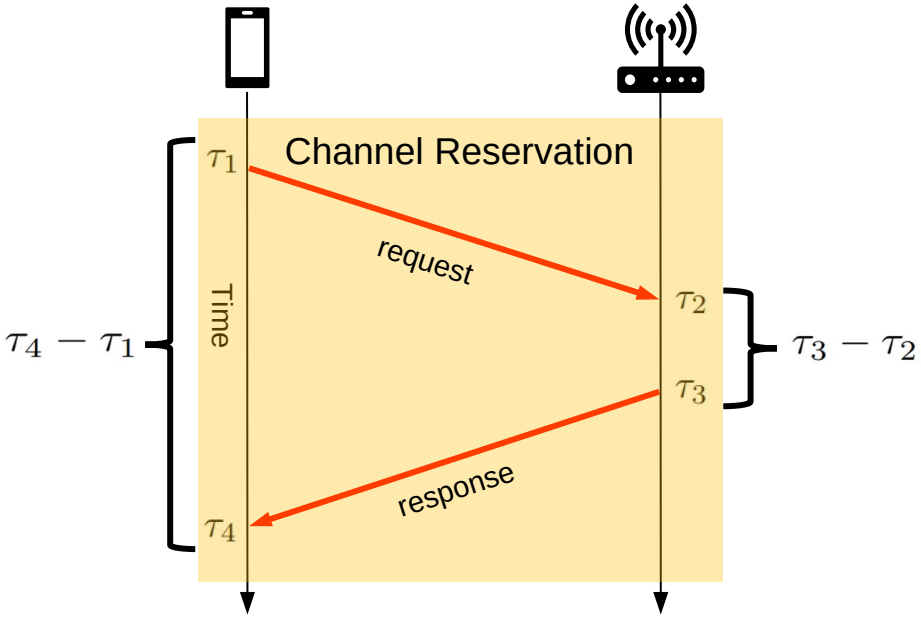


Low-Interference

Wireless Synchronization - The Basic System



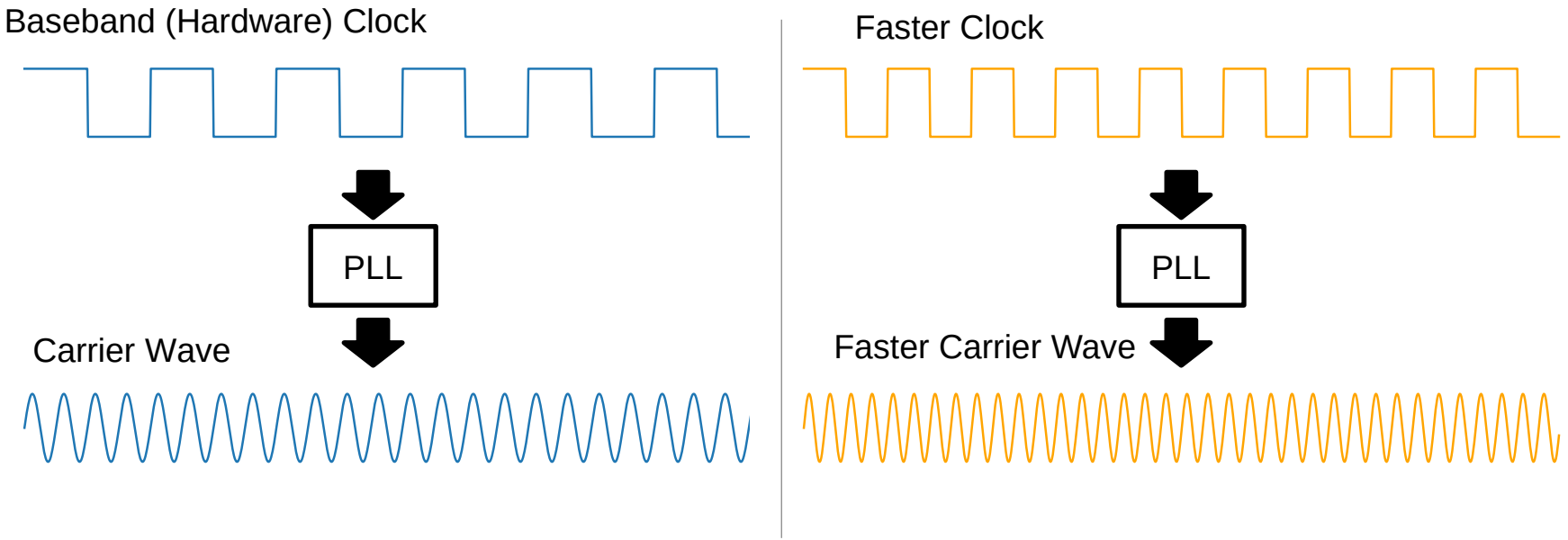
Existing Algorithm - Fine Timing Measurement



$$Delay = \frac{(\tau_4 - \tau_1) - (\tau_3 - \tau_2)}{2}$$

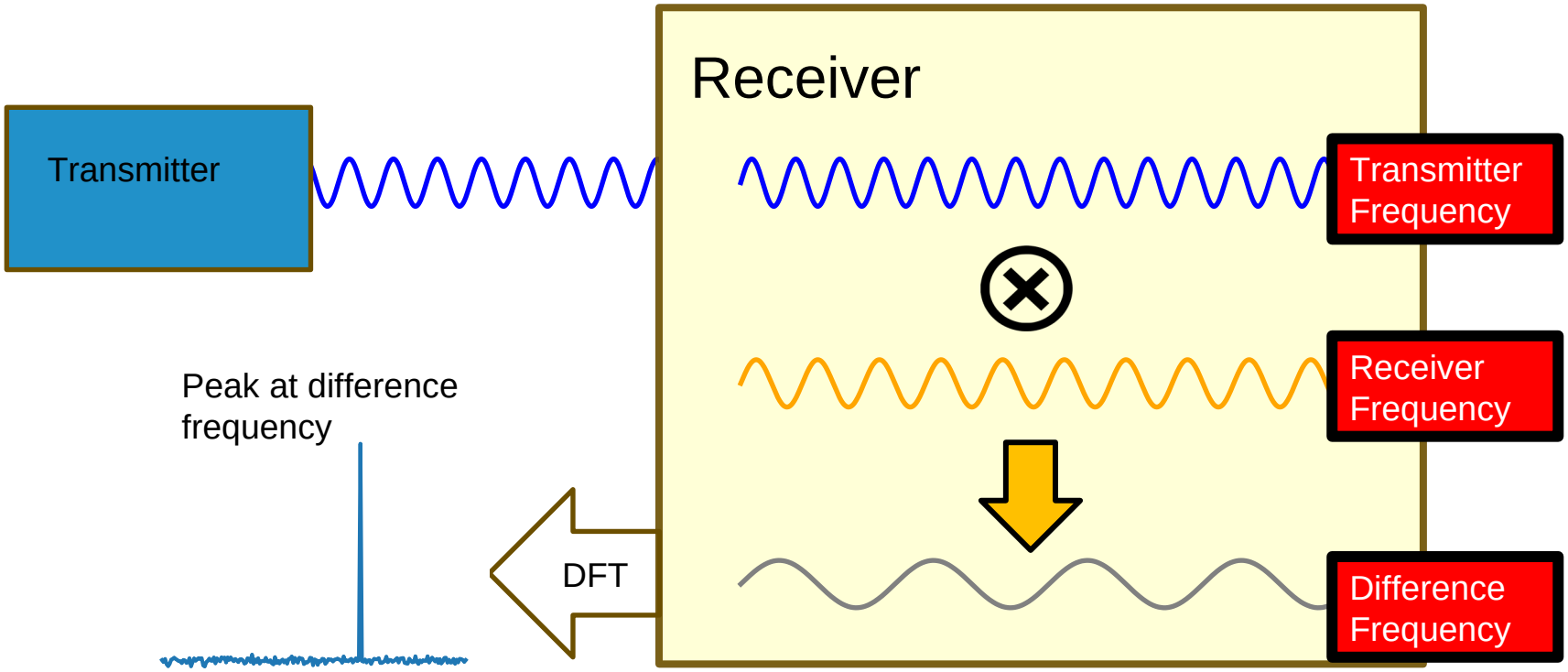
- Time Offset ✓
- Low Overhead ✓
- Feedback ✓
- Frequency Source ?

Frequency offset can be measured with Wi-Fi

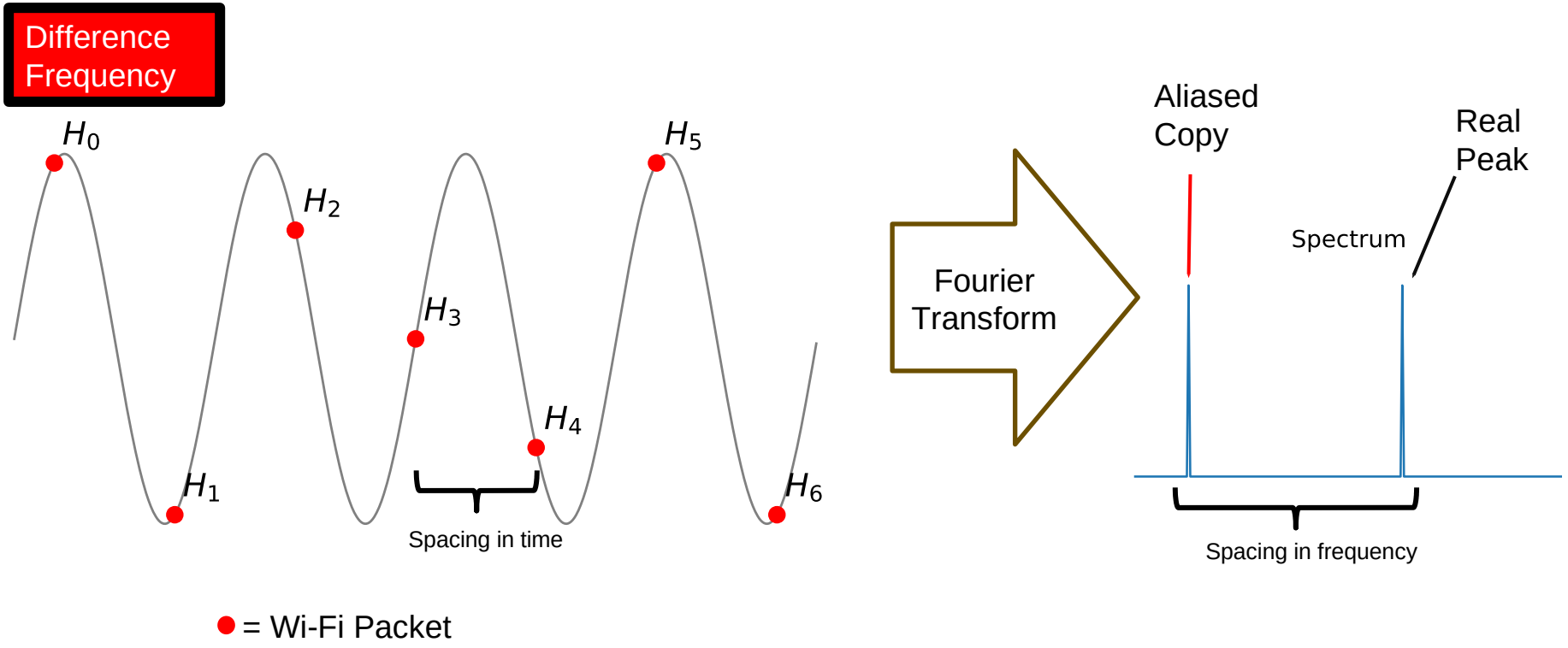


Difference in carrier frequency is difference in clock frequency

Measuring Carrier Frequency Offset (CFO)



Measuring CFO – Aliasing



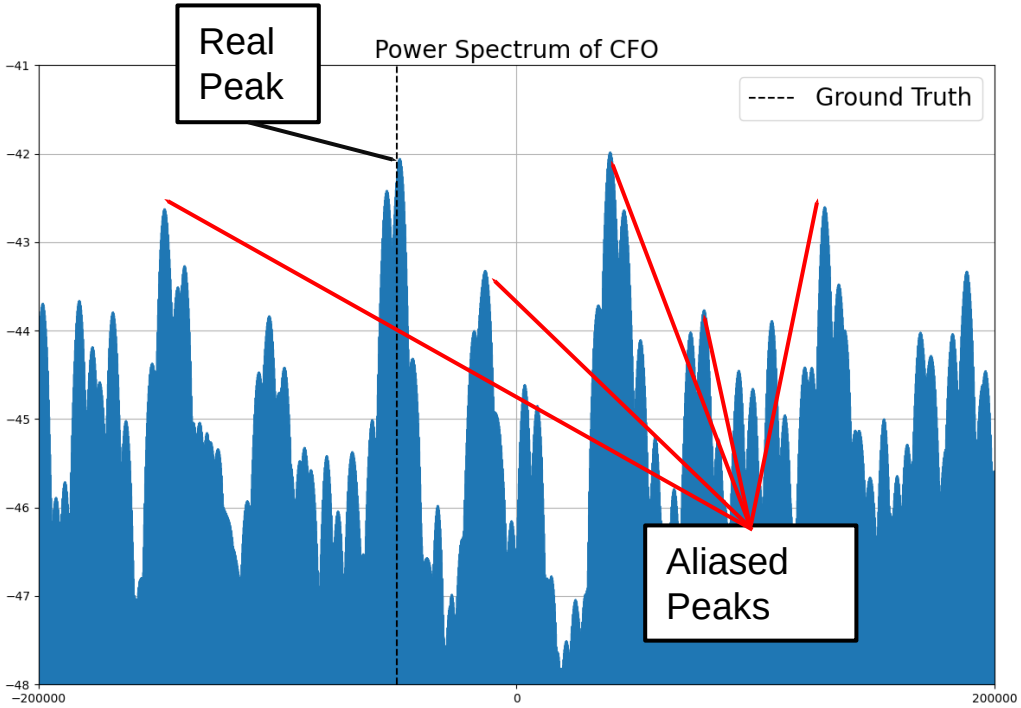
Aliasing Corrupts CFO Measurement

With Aliasing

Closest possible packet spacing ~500μs

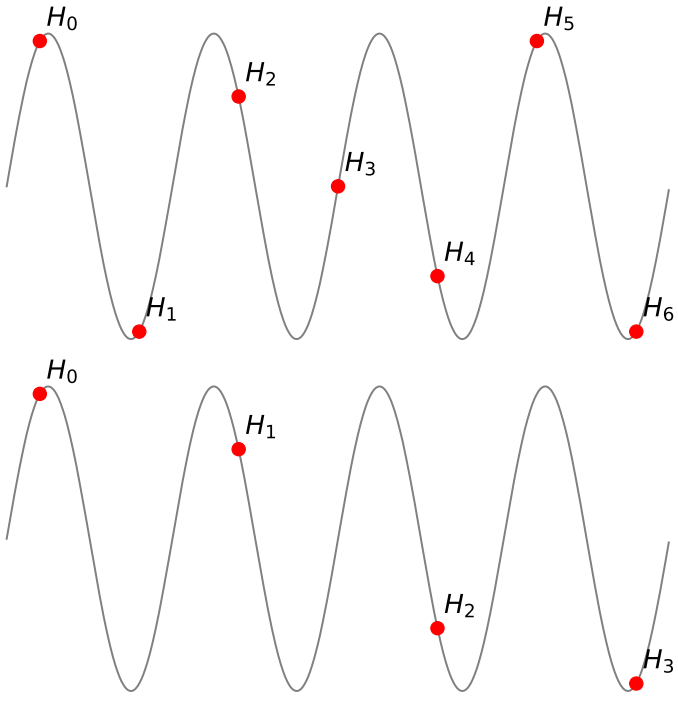
Can measure up to ±1kHz (0.4ppm@2.4GHz)

How can we do better?

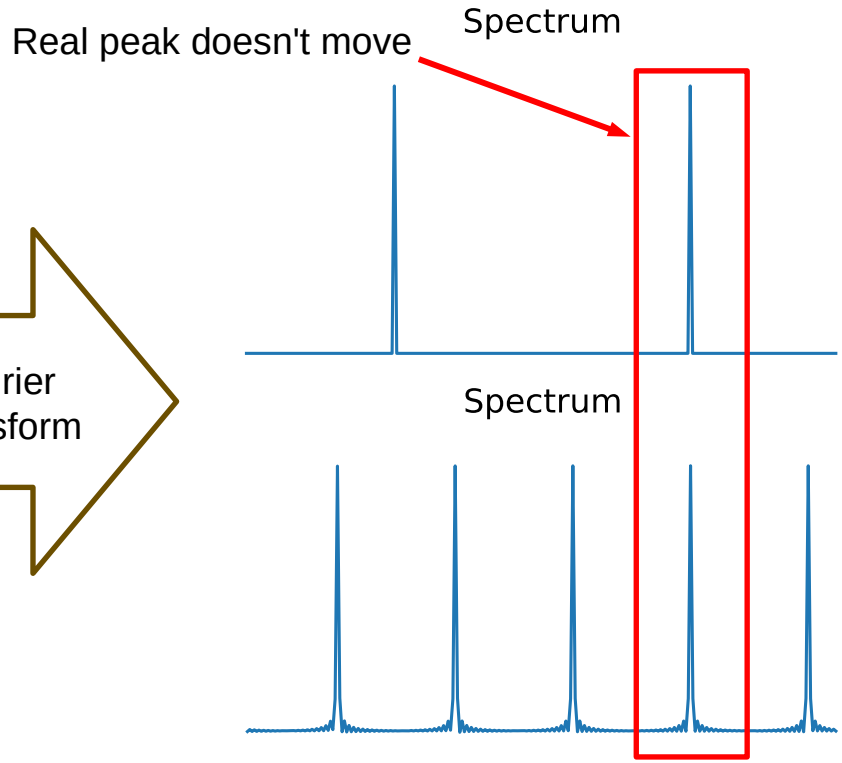


(Aliased peaks are spread + attenuated due to packet arrival time noise)

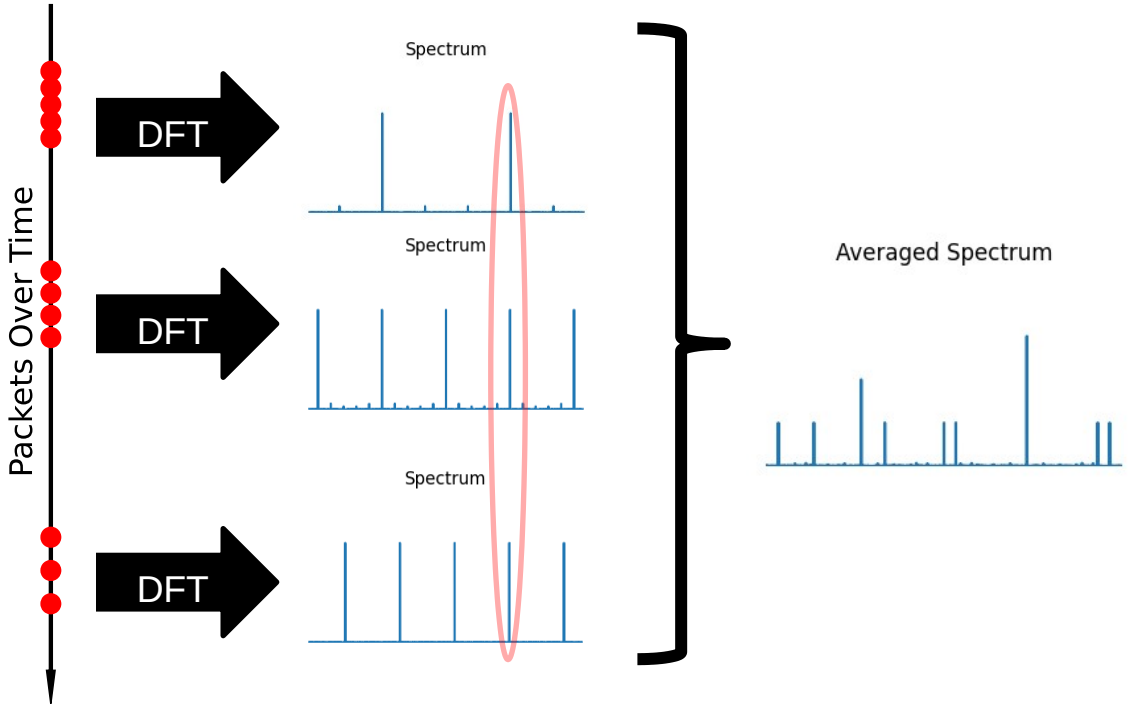
Cancelling Aliased Peaks



Fourier Transform

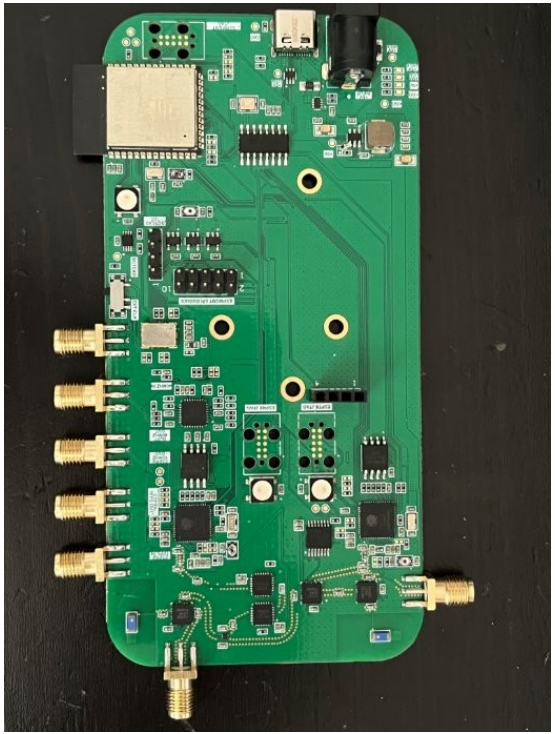


Alias Cancellation

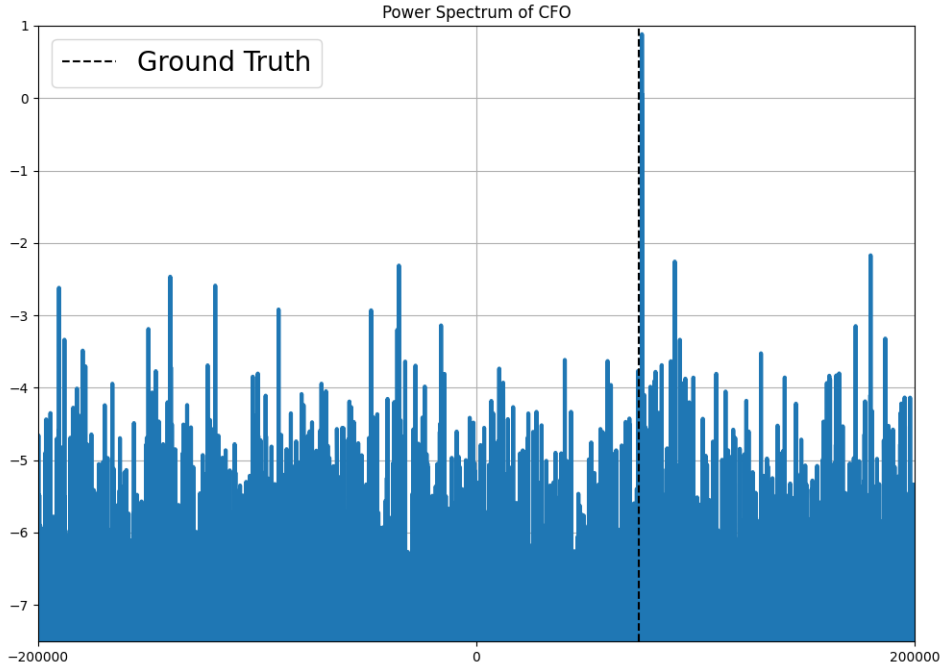


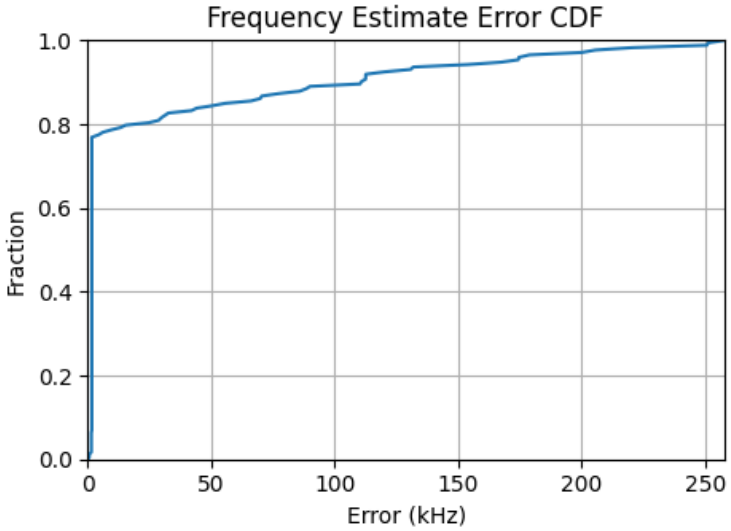
Implementation

- 2x ESP32-S3 WiFi Chipset
- Digitally-Controlled Oscillator
- Experiment: 30 packets over 10 seconds
- 4 packet bursts, 500-1500μs apart



Results

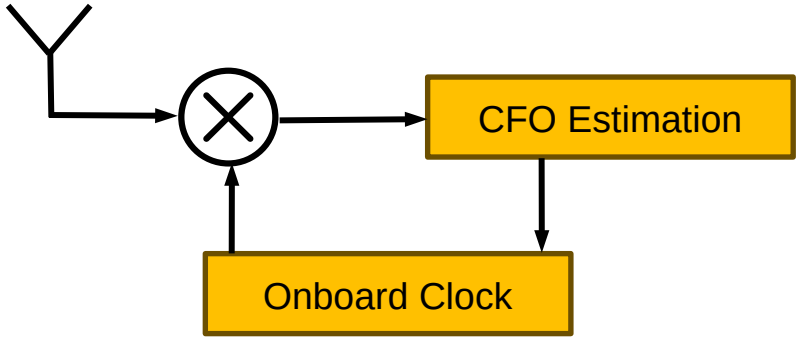

Power Spectrum of CFO
Ground Truth
1
0
−1
−2
−3
−4
−5
−6
−7
−200000
0
200000


Frequency Estimate Error CDF
Fraction
1.0
0.8
0.6
0.4
0.2
0.0
0
50
100
150
200
250
Error (kHz)

Next Steps

Future Work:

- Implement our system alongside FTM protocol
- Use ESP32 DSP hardware to run CFO estimation on-chip



Collaboration:

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Nobu Shiga (shiga@nict.go.jp)