ELECTRONICS & DEFENSE

Software-defined timing: embedded timing for next-generation communication systems

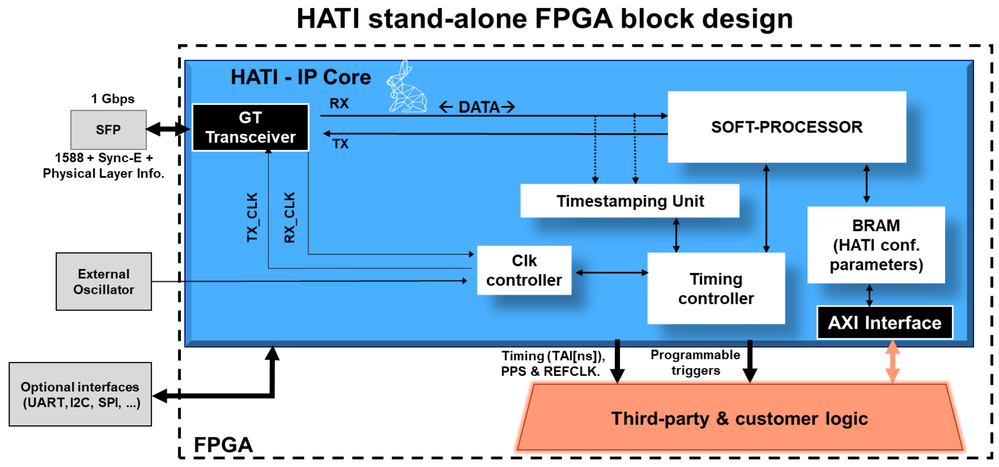
Full programmable functionality is already a reality in today's modern FPGA technology. This facilitates the rapid adoption of technologies such as software-defined radio or networking systems and their implementation in embedded platforms.
In this contribution we present the next generation of timing solutions based on the exploitation of the full programmability of the FPGA towards the software-defined timing paradigm. A standalone White Rabbit/High Accuracy Timing IP (HATI) core is presented as reference example using only FPGA devices resources (not any external clocking circuitry is required). HATI implements the IEEE-1588-2019 High Accuracy (White-Rabbit) protocol to provide sub-nanosecond timing transfer over Ethernet links on third-party enabled devices requiring just optical Ethernet interfaces. The key design considerations, performance, design trade-offs and some key use cases are here analyzed.

#Trustable #Resilient #rPNT #HighAccuracy #FollowTheWhiteRabbit

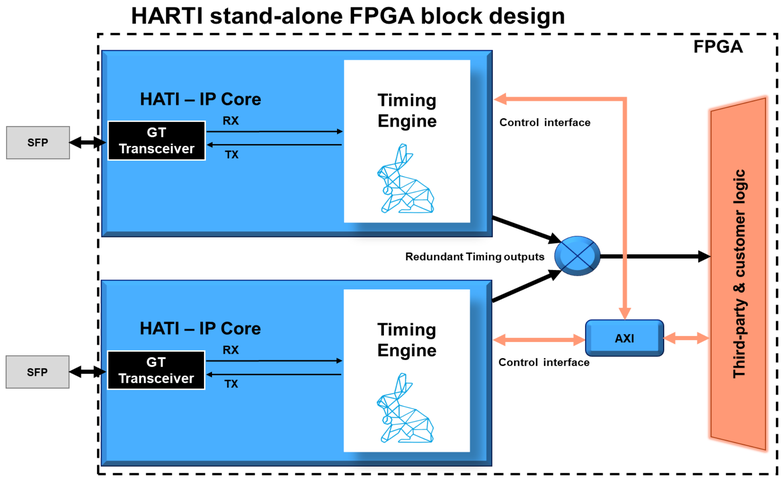
Key features

- Time-transfer software defined solution using only built-in FPGA resources and an optical fiber Ethernet interface
- Resilient configurations are possible by adding redundant HATI cores (HARTI) combined with a timing outputs controller
- Target applications: datacenters, fintech, telecommunications and industrial time transfer
- External management and configuration interfaces allow configuration, calibration, reading IP status
- Adapted to ensure picosecond-level determinism with transceivers from multiple FPGA families

HATI stand-alone FPGA block design



HARTI stand-alone FPGA block design



Requirements

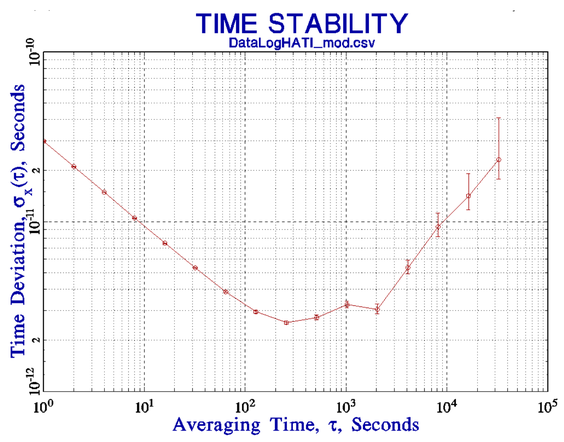
- The HATI must be physically connected to an SFP cage outside the FPGA
- The HATI core needs a 125 MHz clock coming from an external source and the clock must be routed to the FPGA Gigabit Transceiver clock pins
- One general purpose FPGA pin must be directly connected to some external coaxial connector (SMA or equivalent) for calibration
- One time calibration is needed when a new HATI FPGA binary is generated
- It is recommended to use the HATI along with a hard-processor (Zynq SoCs or external ARMs) for operation

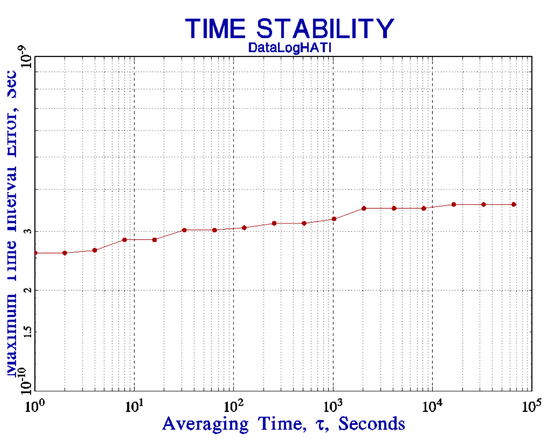
HATI FPGA interface and resources (reference prototyping FPGA)

Resource	Used	Available	Utilization %
LUT	14404	171900	8.38%
Registers	14102	343800	4.1%
BRAM	82	500	16.4%
DSP	6	900	0.67%
MMCM	2	8	25%
PLL	2	8	25%

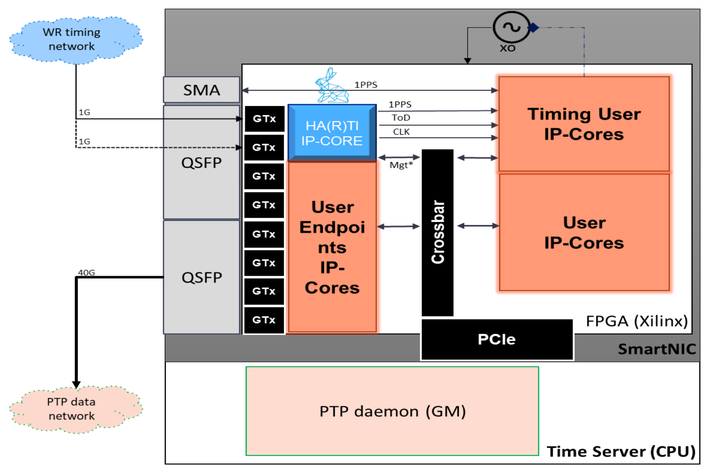
HATI reference design based on prototyping board

HATI MTIE AND TDEV RESULTS





Use case example. HATI enabled SmartNIC



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