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An Architecture to Stamp Asynchronously the TOD with 1 ps Resolution

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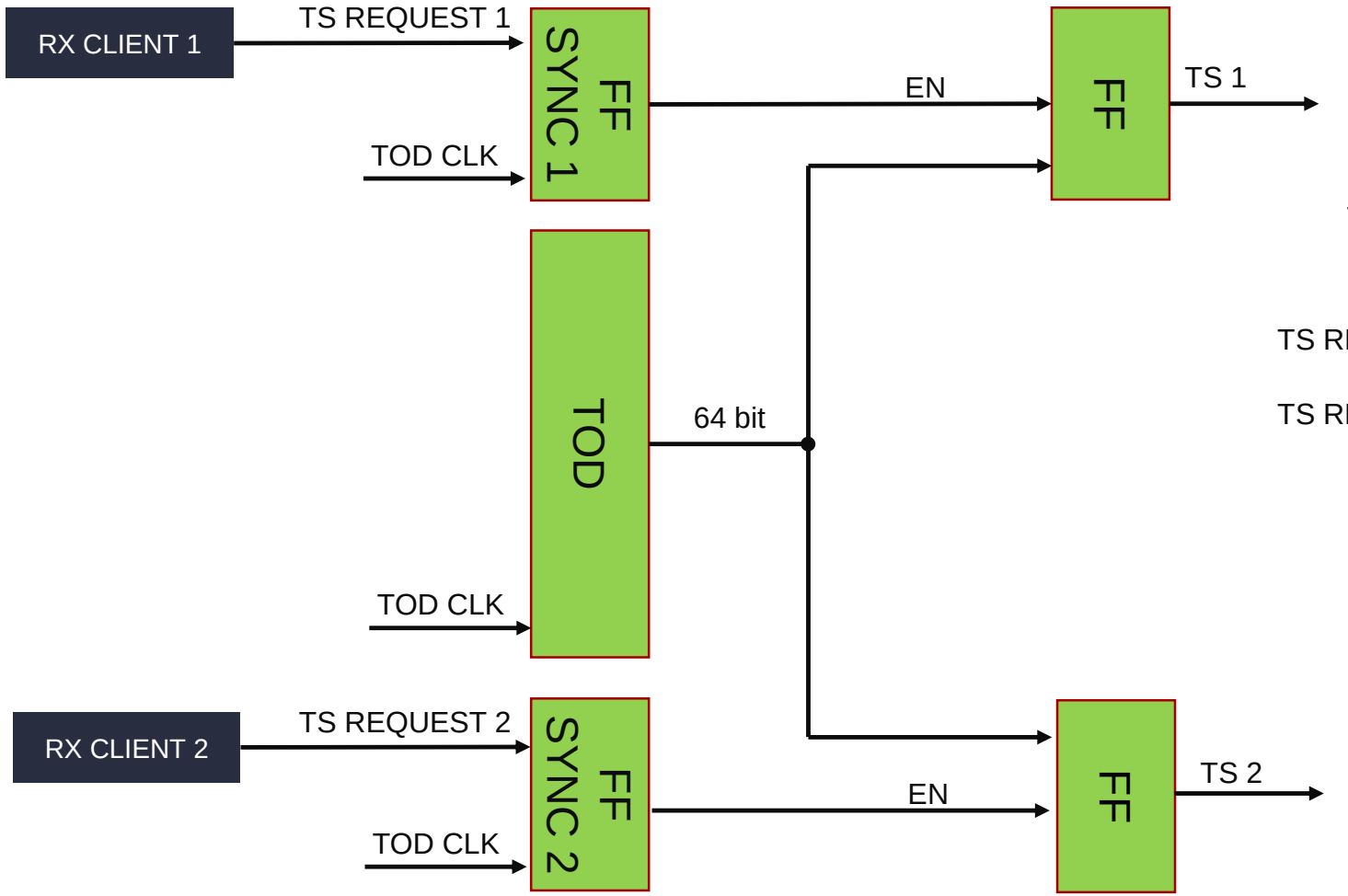
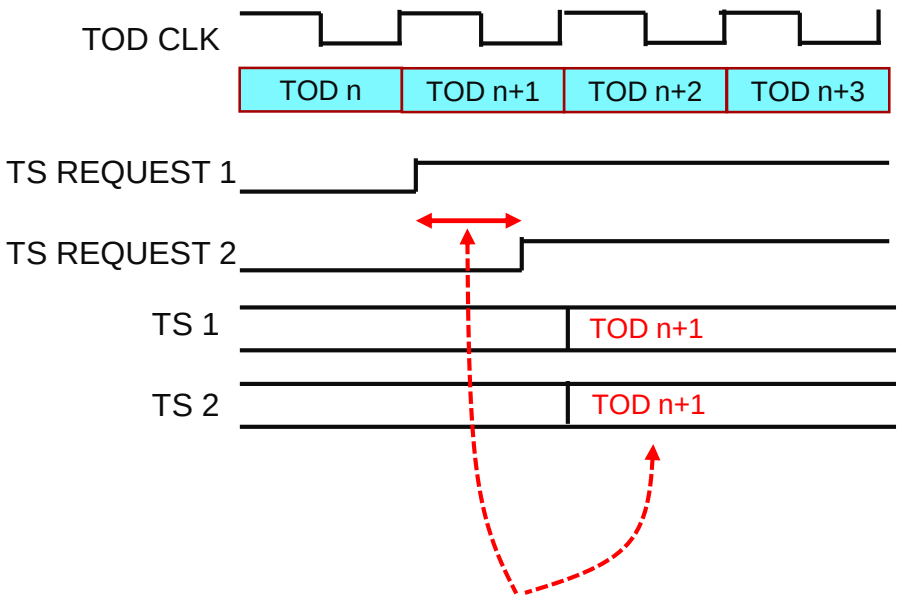
- Introduction
- The Problem of Stamping the TOD
  - Solutions based on classical methods
- New Architecture
  - Advantages
- Conclusion

The Problem: Stamping the TOD





Phase difference of TS REQUESTS
Is not reflected in the TS

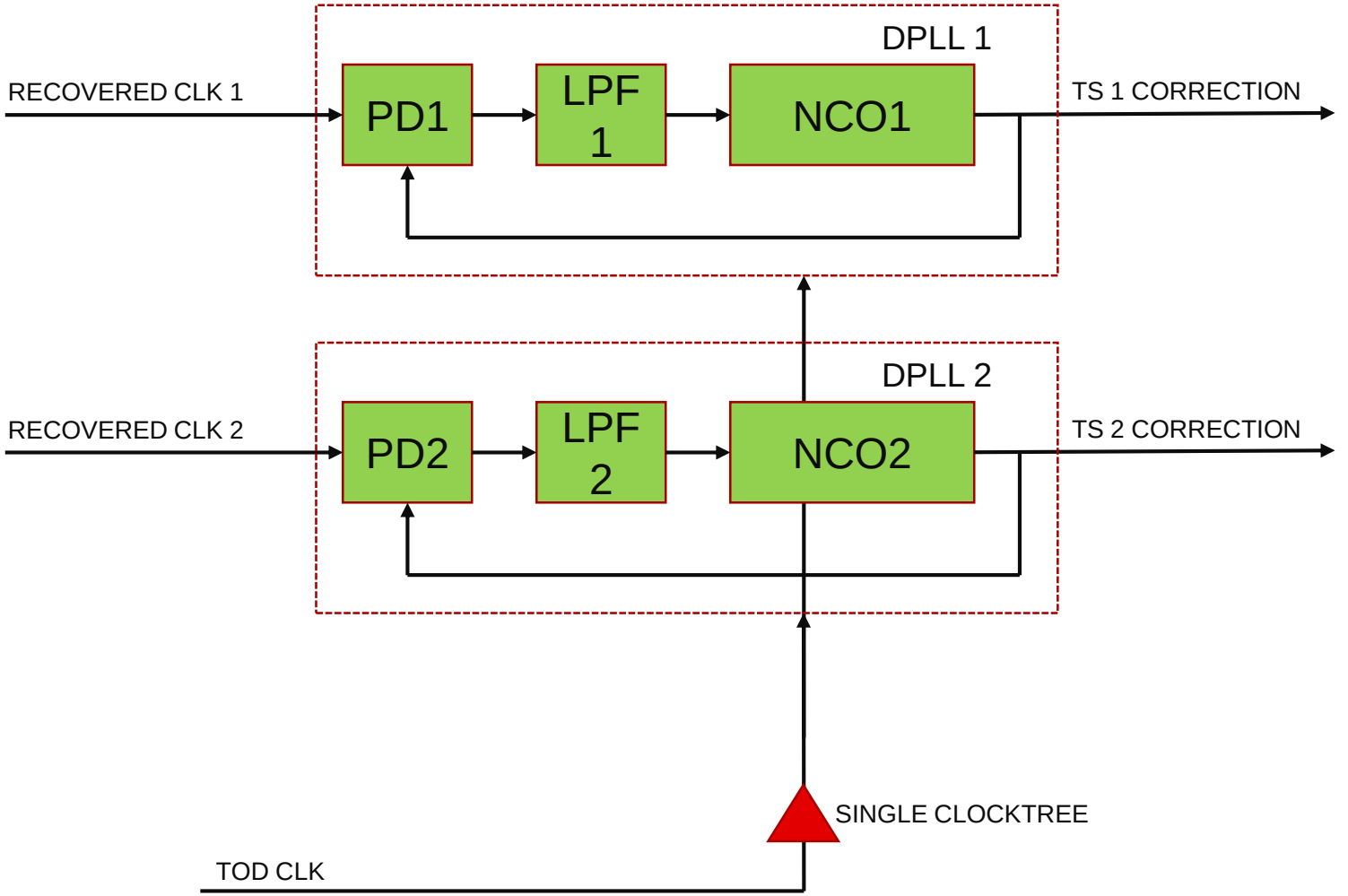
TOD sampling error: TS 1 and TS 2 are equal, althogh there is a phase difference between TS REQUEST 1 and 2

Classical Solutions

- Increasing the TOD clock frequency
- Generating a polyphase TOD.

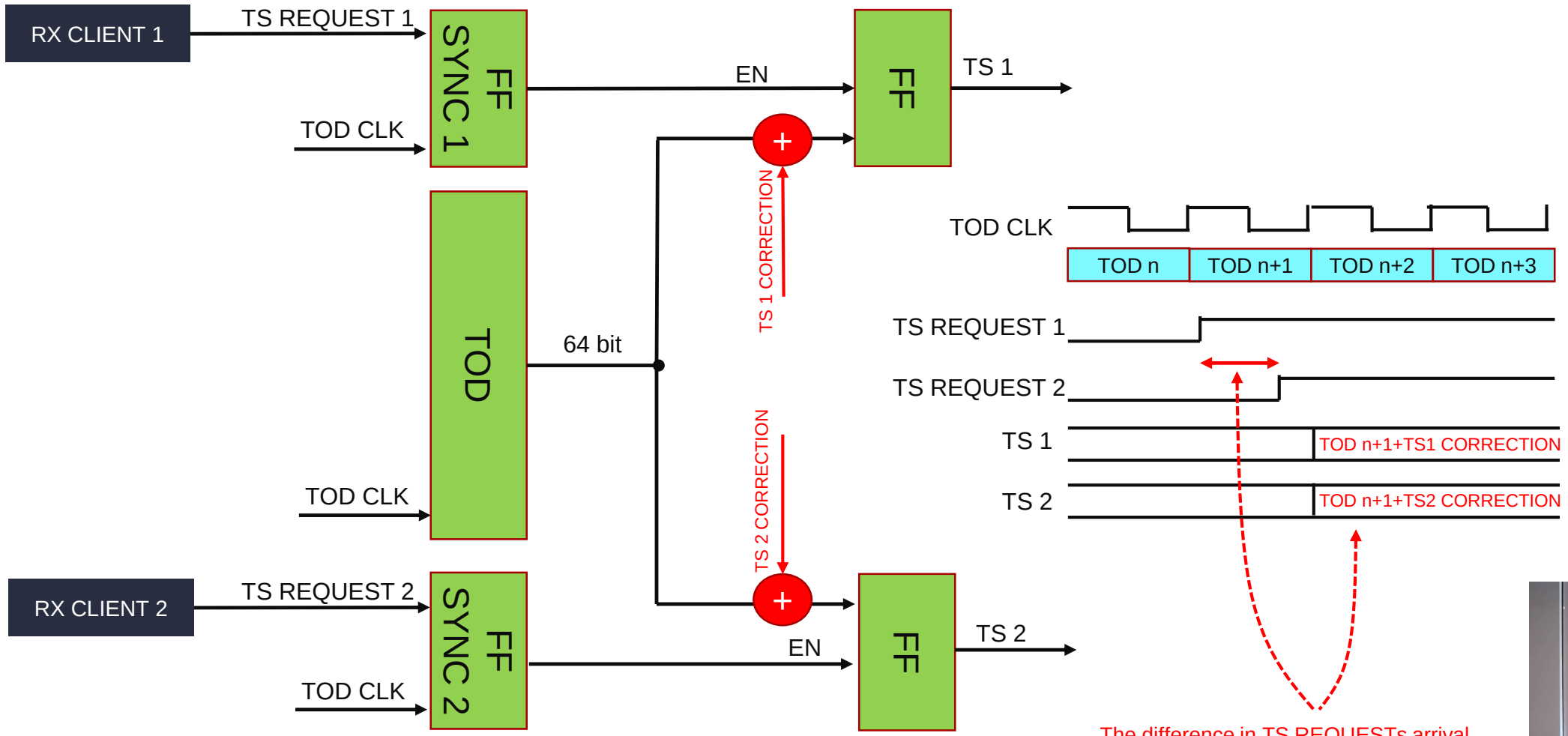
Improvement is limited by silicon technology

Architecture



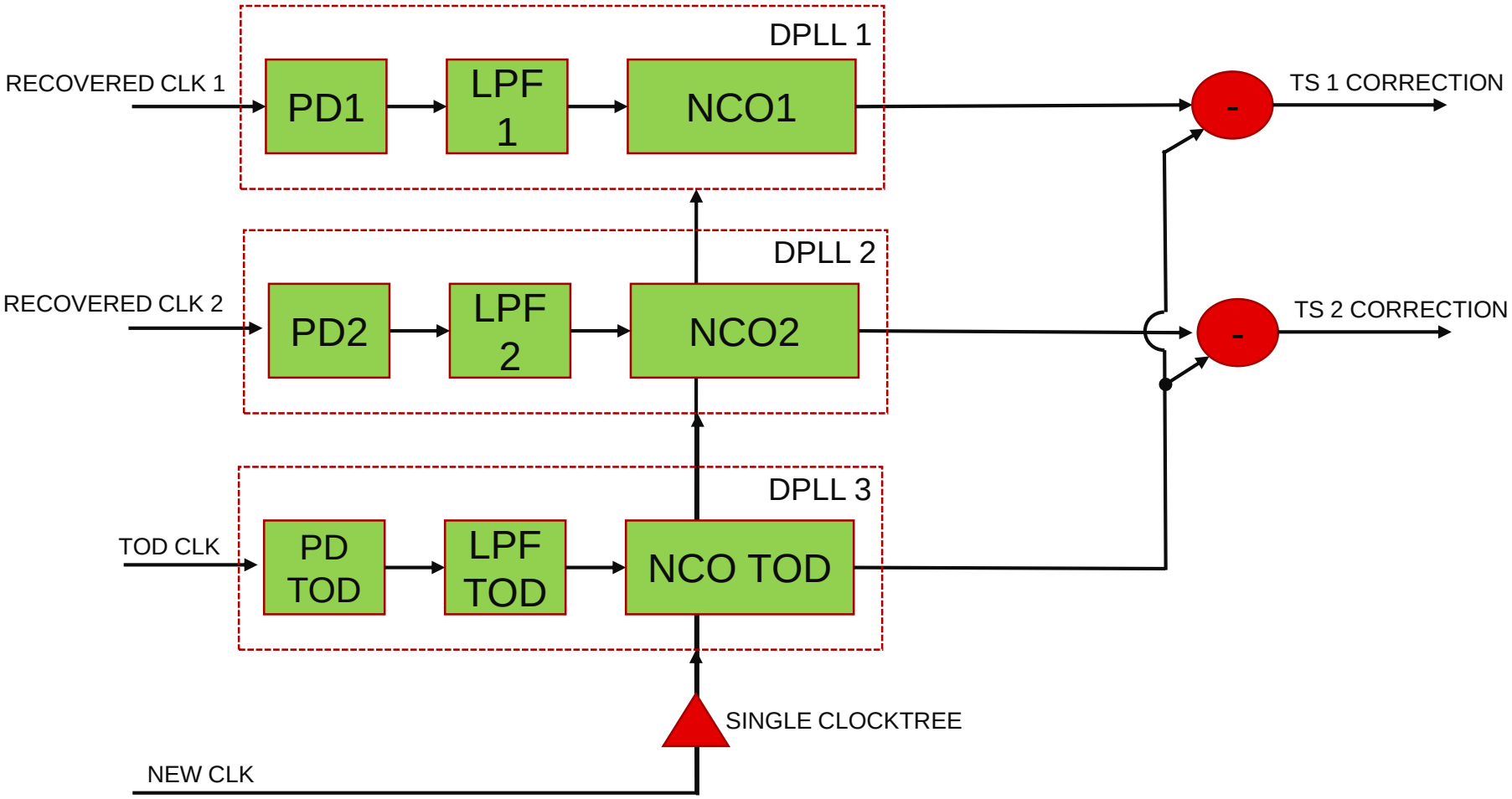
Improvement is limited by Architecture

Precise TOD Stamping: Architecture



The difference in TS REQUESTs arrival
Is reflected in the time stamps.

Synchronous TOD Clock



Conclusions

- The electronics plays a role in the precision and accuracy of the overall TOD stamping
- Focus on DSP architectures to improve precision in asynchronous TOD stamping.
  - Paradigm shift: focus on architecture vs focus on silicon technology
- This architecture is very suitable for programmable hardware – FPGA.

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Thank You