Practical Implementation of a IEEE 1588 Based Synchronization Distribution System

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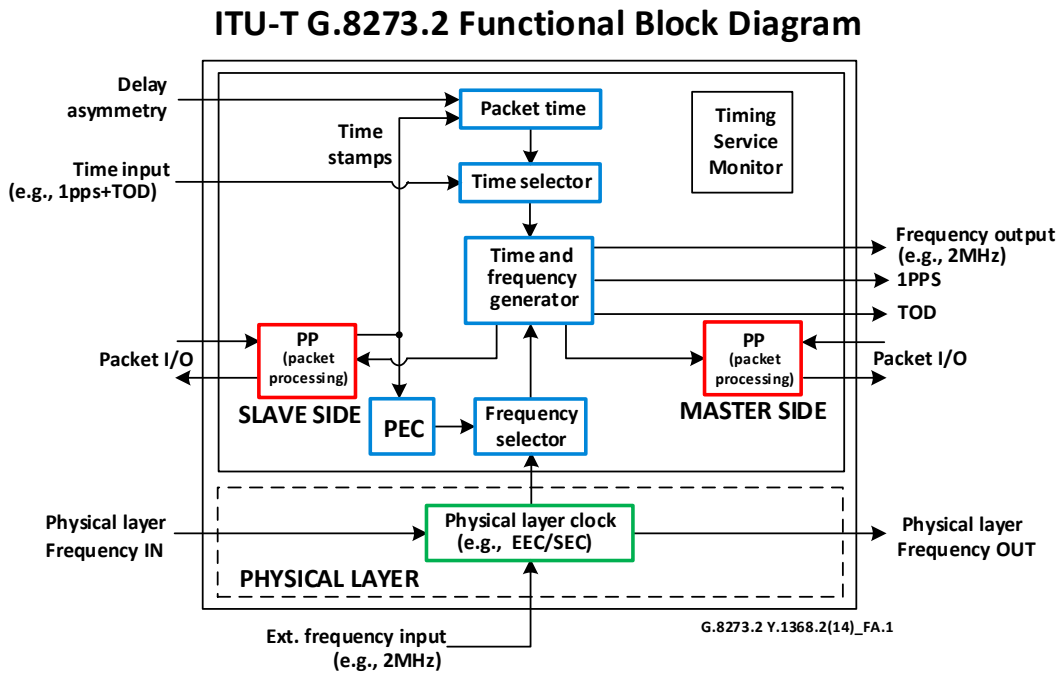
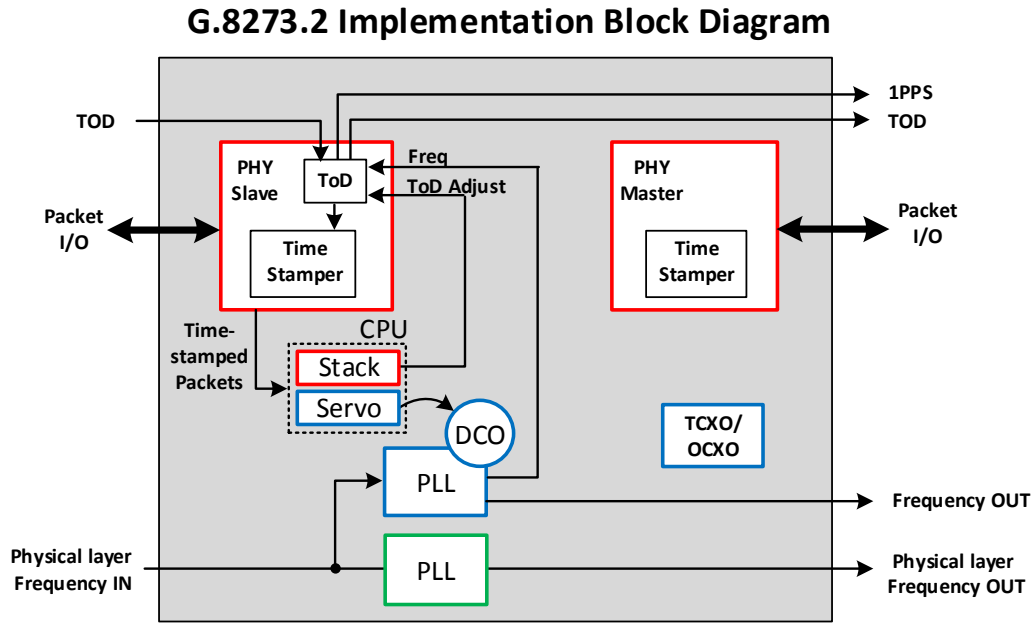
Agenda

- Practical Implementation of a T-BC
- ToD Synchronization Between Master and Slave
- ToD Synchronization within the Network Element
- Challenges of Meeting 5ns Time Error
- Possible Solutions for Meeting 5ns and Beyond

Implementation of a Telecom Boundary Clock (T-BC)





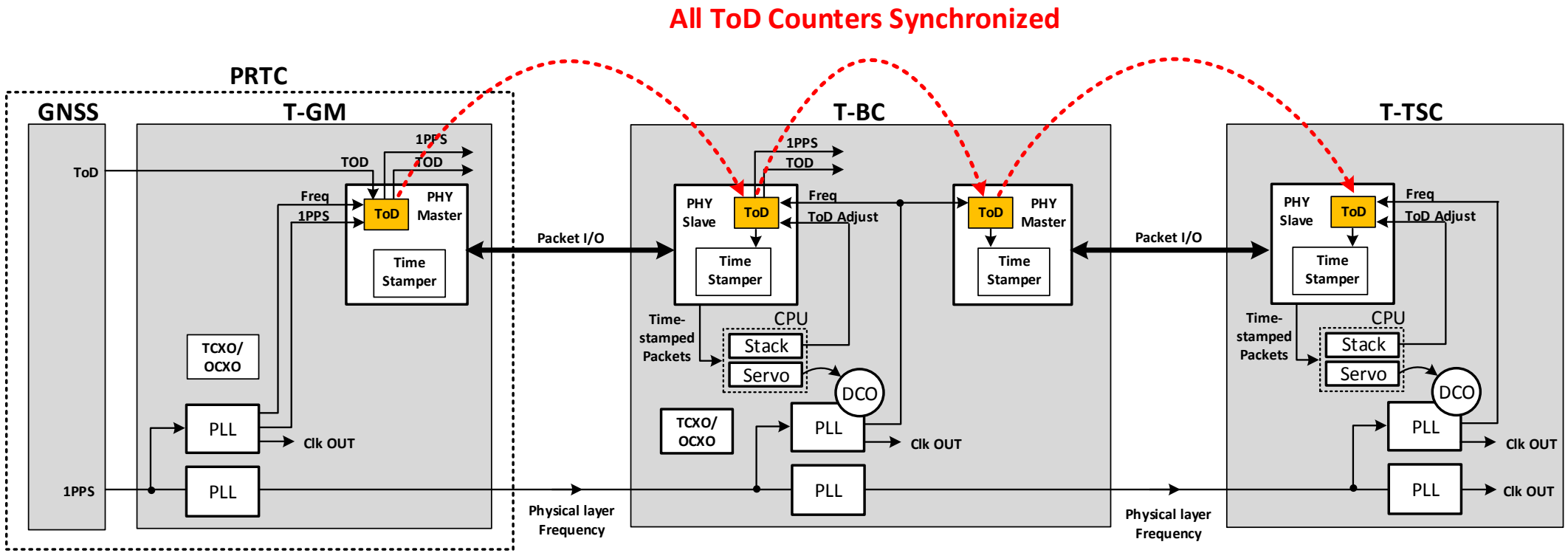
Main functions of a T-BC:

- Packet processing (PTP stack, timestamping)
- PEC (uses timestamps to generate clocks)
- Physical layer clock (unaltered by PTP)

Main physical components of a T-BC:

- Master and Slave PHY (ToD/timestampers)
- Processor (1588 stack & servo)
- 1588 PLL (with DCO)
- SyncE PLL (independent from 1588 PLL)
- TCXO/OCXO (for frequency stability)

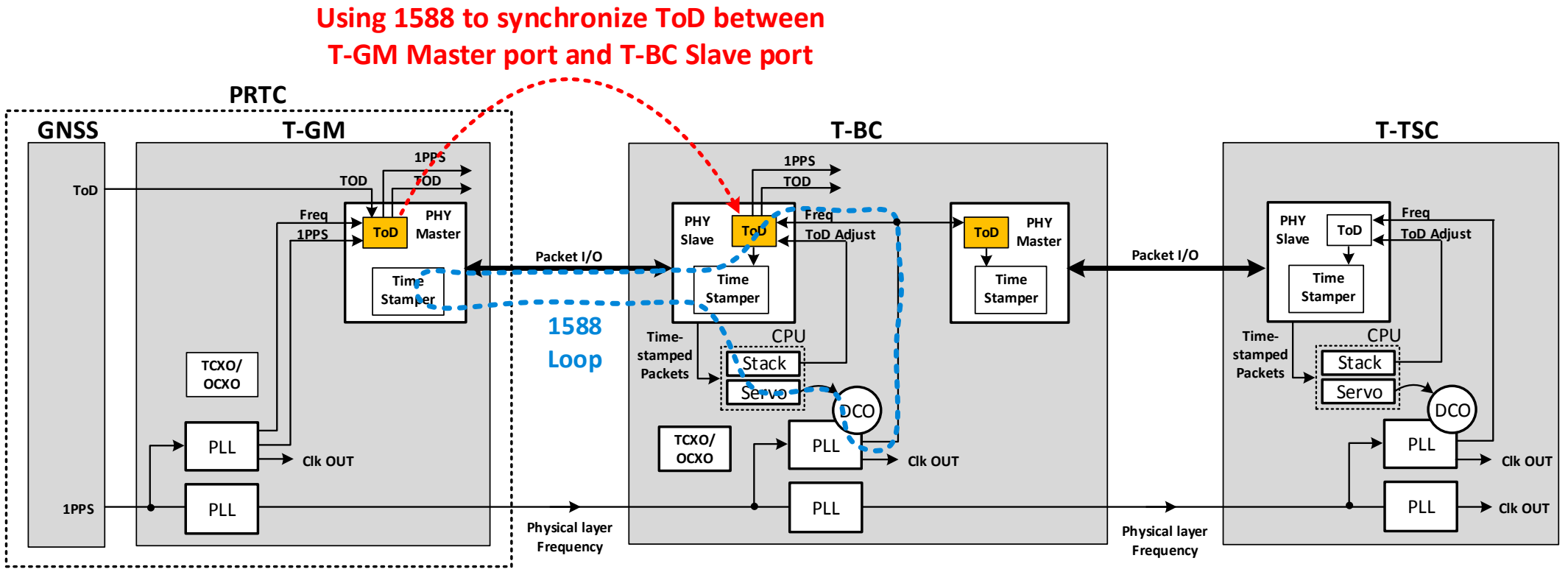
The Goal of Network Synchronization



All ToD counters within the timing chain must be synchronized with the T-GM:

- They contain the same time value
- They turn over at the same time (with nano-second accuracy)

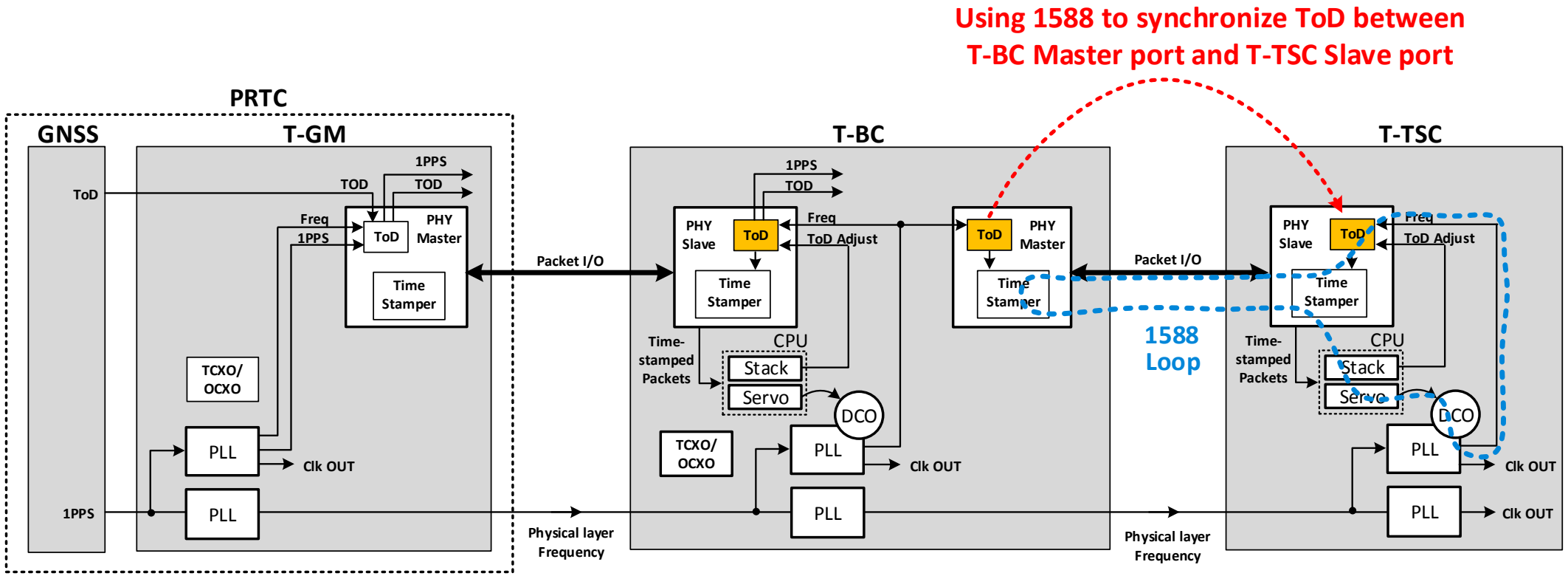
T-GM to T-BC ToD Synchronization



Three stages of ToD synchronization:

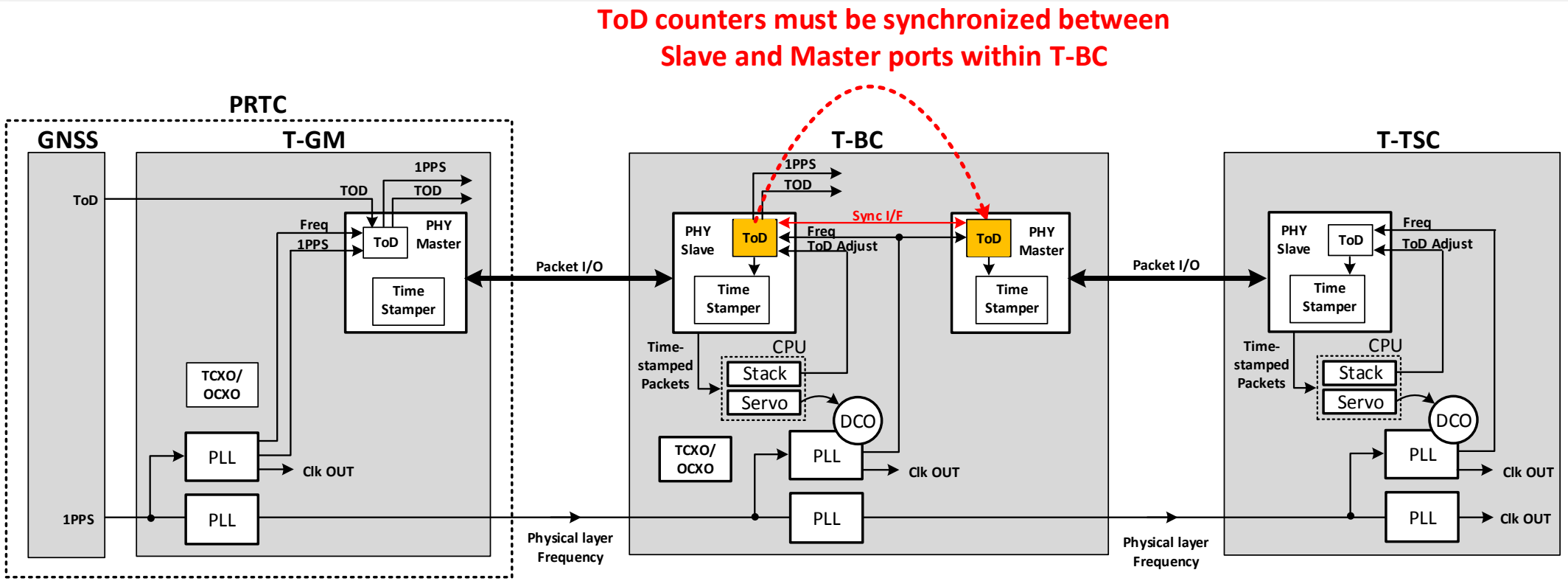
1. Initial adjustment: T-BC extracts ToD from 1588 packet sent by T-GM
2. Lock acquisition: T-BC servo uses timestamp information to adjust ToD counter frequency minimizing time error
3. Locked: T-BC servo makes fine adjustments of ToD frequency to keep time error at zero

T-BC to T-TSC ToD Synchronization



- **T-TSC:** Slave port synchronizes its ToD to upstream T-BC master port
- **T-BC:** It is critical that ToD at slave & master ports are perfectly synchronized…

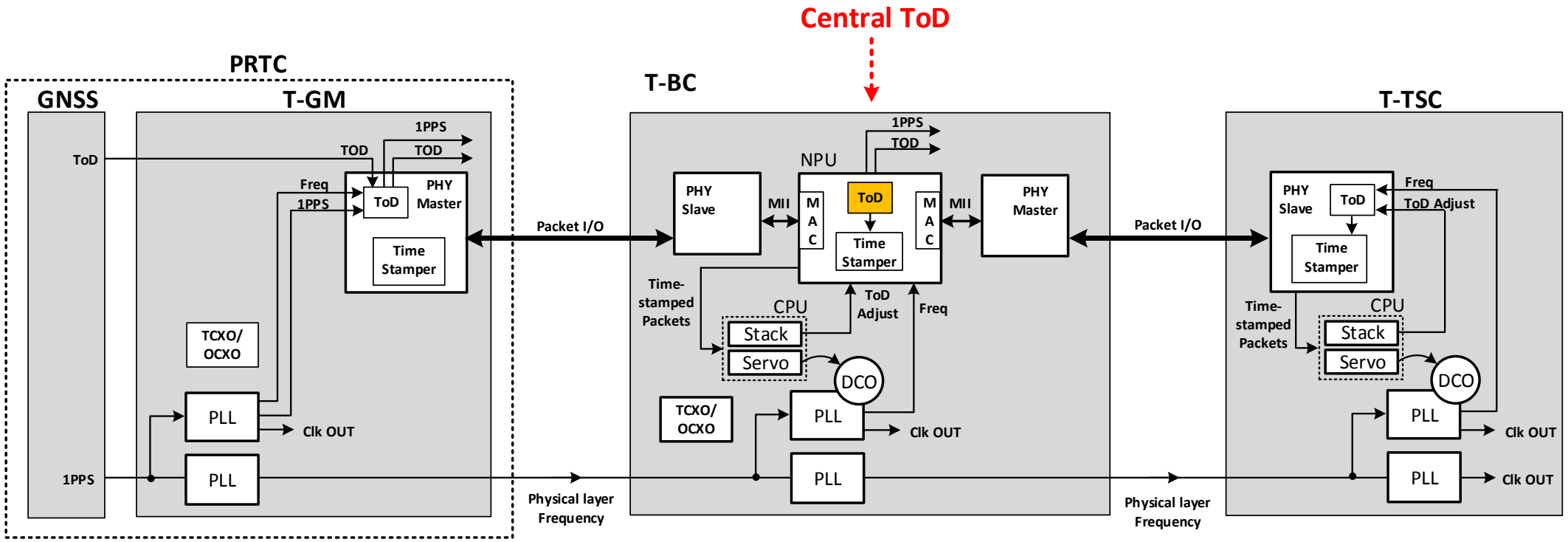
Option 1: T-BC ToD Synchronization –> Using a Physical Interface



If timestamping is performed in separate physical locations within the T-BC…

- Synchronization of ToD at slave and master ports must be synchronized (or it will contribute to time error)
- Proprietary interfaces help ToD synchronization between PHYs

Option 2: T-BC ToD Synchronization –> Using a Central ToD/Timestamper

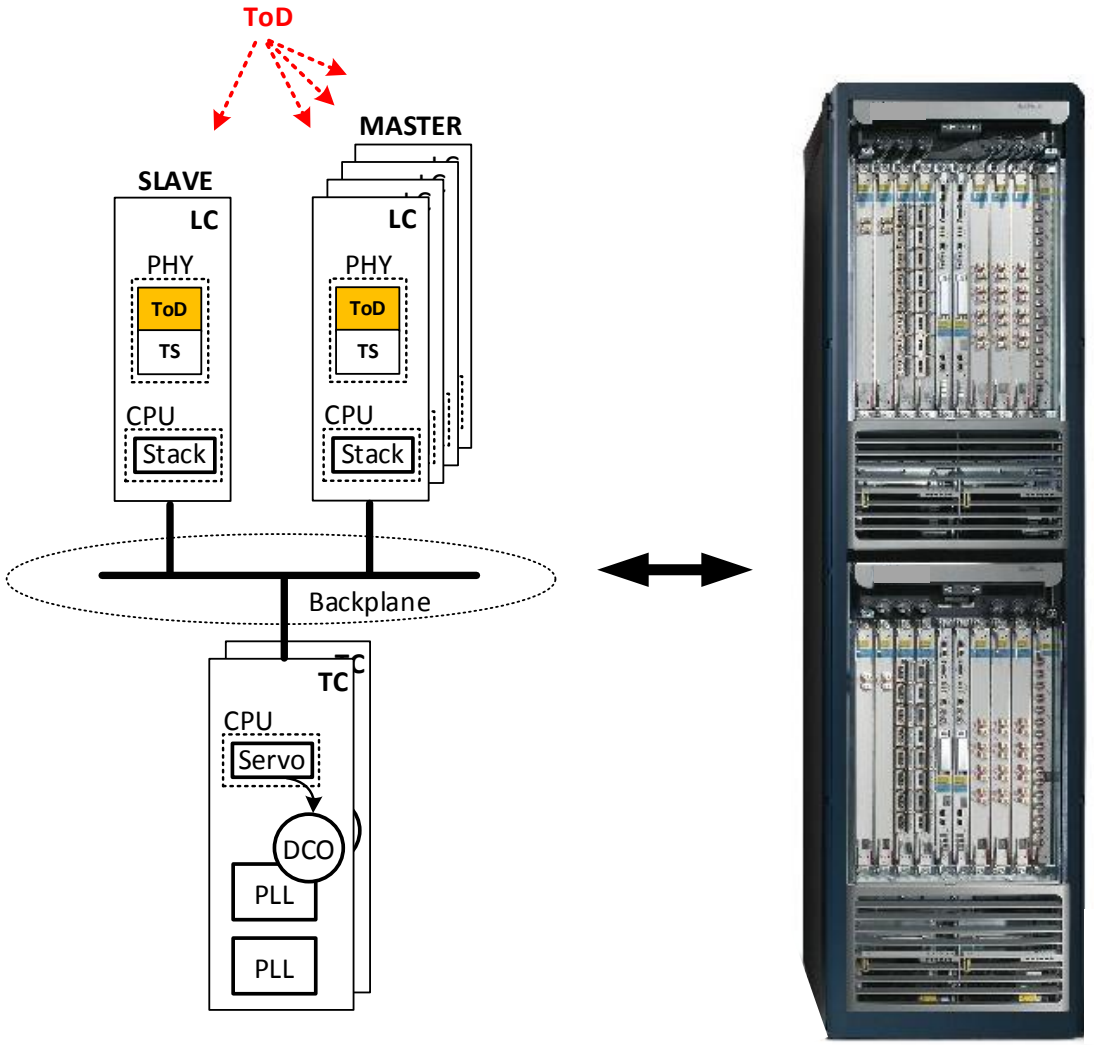


ToD and Timestamping can be located at a central point in the system

- Synchronization of ToD at slave and master ports must be synchronized (or it will contribute to time error)
- **Or** timestampers must reference a central point of ToD…

Multi Circuit-Pack System Architecture

- Most carrier grade equipment is broken down into multiple circuit packs connected together with a backplane
- Timestamping/ToD and PTP stack functions (Line Card) are separated from the central clock generation functions (Timing Card)
- There's still a need to synchronize ToD from the slave line card to ToD of master line cards



Distribution of ToD across a Multi Circuit-Pack System

ToD Distribution

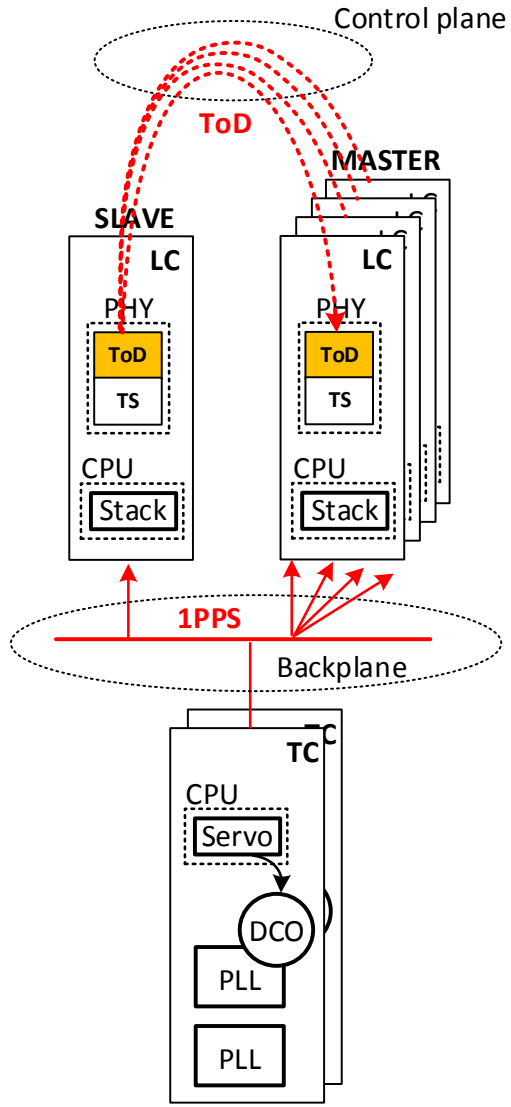
- ToD from Slave line card is distributed to all Master line cards
- ToD is distributed over control plane
- Precision not important (1 second to get there)
- 1PPS provides ToD 1-second rollover precision

1PPS Distribution

- 1PPS is generated by PLL/DCO (controlled by 1588 Servo)
- Objective is to align all 1PPS signals across all line cards
- Any 1PPS phase misalignment looks like time error

Challenges

- Backplane trace lengths must be matched or compensated
- Delay uncertainty of backplane drivers/receivers must be considered in timing budget
- I/O delay of line card PLL must also be considered



Solution 1: Manual Calibration of 1PPS Distribution Path

Backplane Trace Delays

- 1PPS backplane trace delays are manually measured
- Variance in PCB trace length during manufacturing causes delay uncertainty

Backplane Driver/Receiver Delays

- Driver + Receiver delay uncertainty over PVT : 2-3 ns typ

Line Card PLL

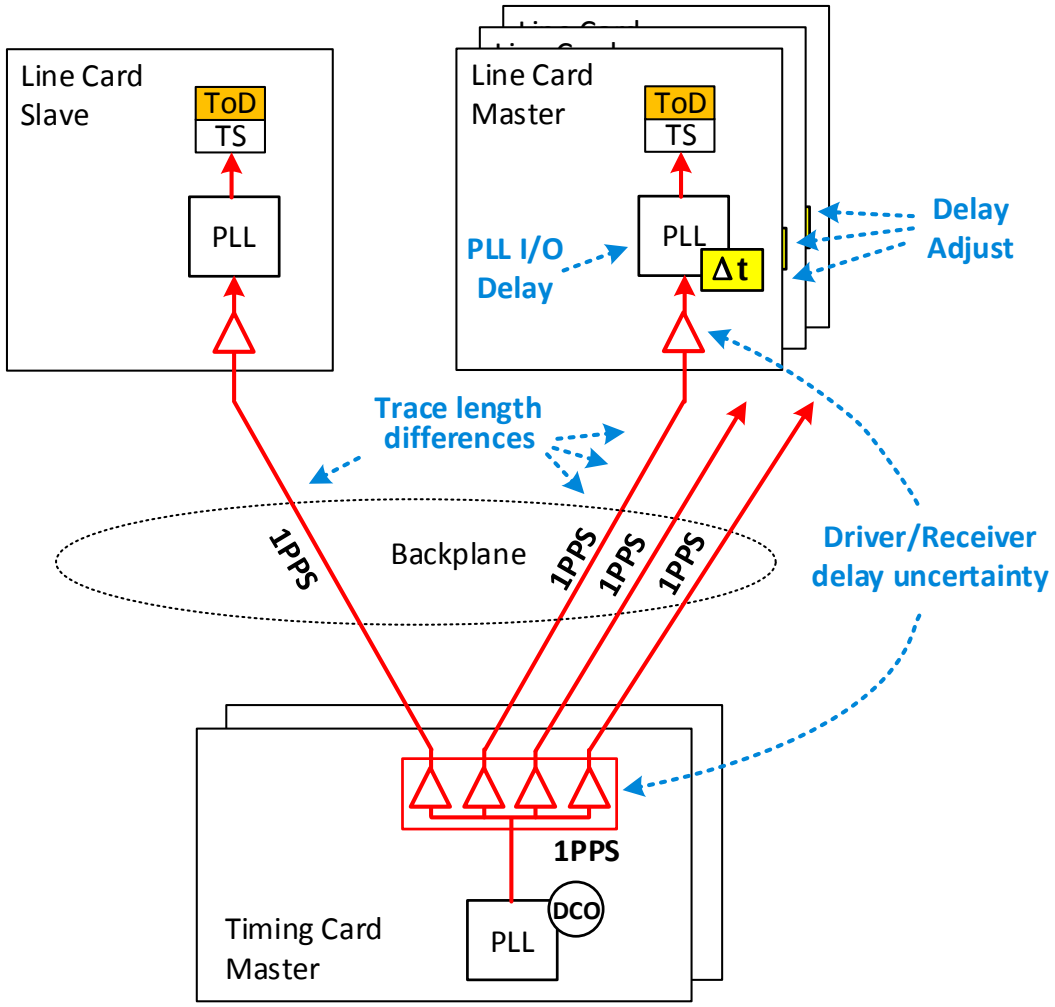
- Keep I-O delay as low as possible by using ZDM
- All deterministic delays can be compensated for using adjustable delay at Line Card PLL.

Challenges:

- Delay uncertainty from PCB traces, drivers/receivers, and Line Card PLL adds to the time error budget
- Drivers/receiver delay uncertainty is the main contributor

PVT - Process/Voltage/Temperature,

ZDM – Zero Delay Mode



Solution 2: On-chip 1PPS Delay Measurement & Adjust

Measuring 1PPS path delays

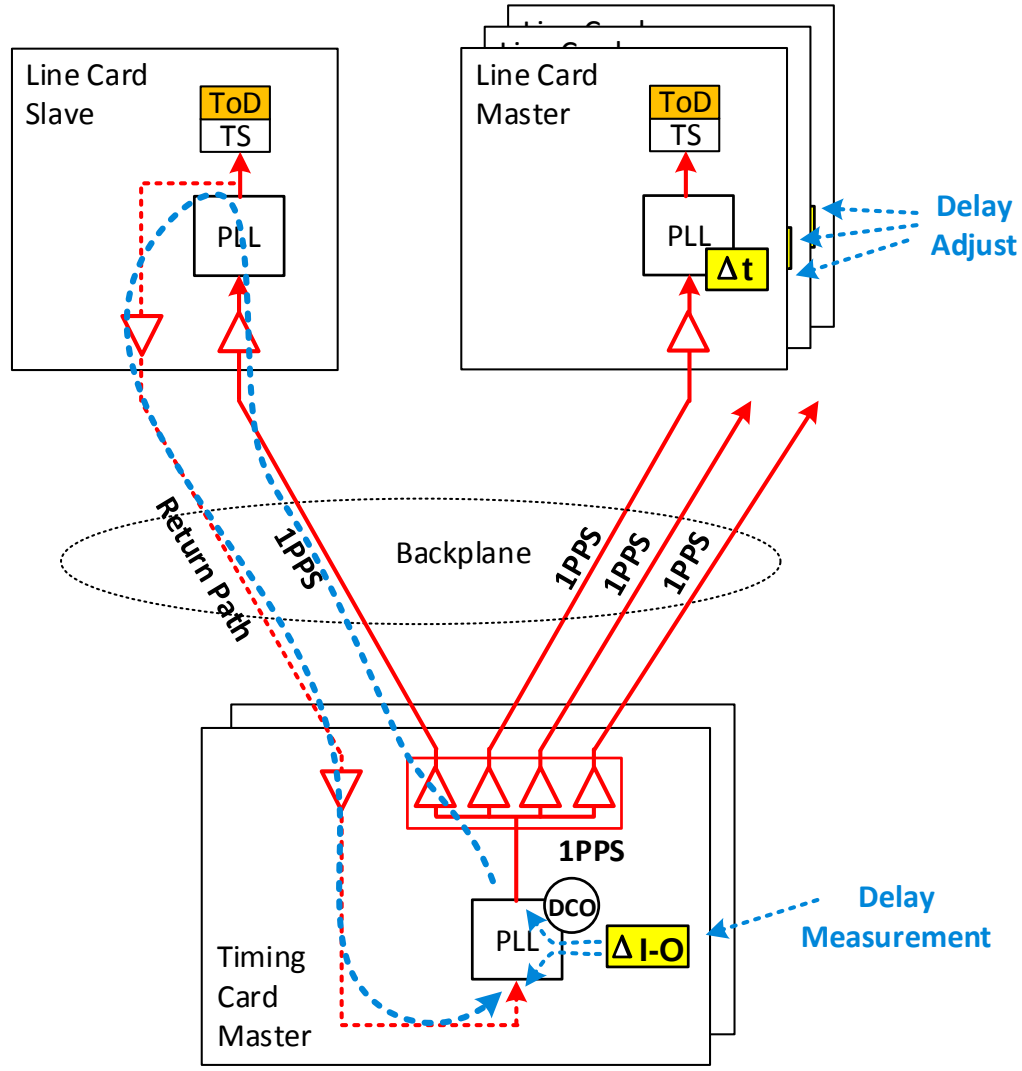
- 1PPS path delays are measured at start-up
- Must be done for each Line Card (each 1PPS path)
- Delay measurement performed at central point in the system. In this case at the Timing Card.
- Could use existing SyncE backplane traces to provide return path
- Measured trace delay differences are adjusted at line cards
- 1PPS delay = Round Trip Delay minus Return Path delay

Advantage:

- Compensates for both backplane trace delay and driver/receiver delay uncertainty

Challenges:

- Assumption that forward and return paths are symmetrical
- Return path must also be measured (using TxSyncE/RxSyncE pair?)



Conclusions

- Time error of a T-BC consist of PTP servo error + misalignment of ToD
- Distribution of ToD in a multi circuit-pack system takes careful design
- Meeting 5ns time error is a difficult challenge.
- New design practices and synchronization distribution architectures will be needed

Thank You